

## SL6408 Data sheet description Ver1.3

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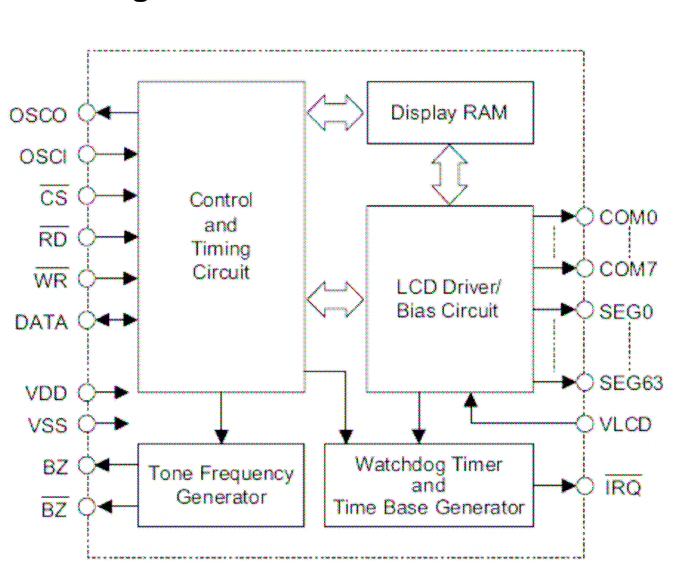
## ● Features

- Operating voltage: 2.4V~5.2V
- Built-in RC oscillator
- External 32.768kHz crystal or 32kHz frequency source input
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 64x8 patterns, 8 commons, 64 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base/WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Cascade application
- EL application (The charging and discharging frequency of EL are adjusted by two external resistors.)

## ● General Description

SL6408 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 384 patterns (64x8). It also supports serial interface, buzzer sound, watchdog timer or time base timer functions. The SL6408 is a memory mapping and multi-function LCD controller. The software configuration feature of SL6408 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the SL6408.

### Block Diagram



Note: CSB: Chip selection  
 IND\_BZ, EL\_BZB: Tone outputs/EL application  
 WRB, RDB, DATA: Serial interface  
 COM0~COM7, SEG0~SEG63: LCD outputs  
 IRQB: Time base or WDT overflow output

## ● Pad Description

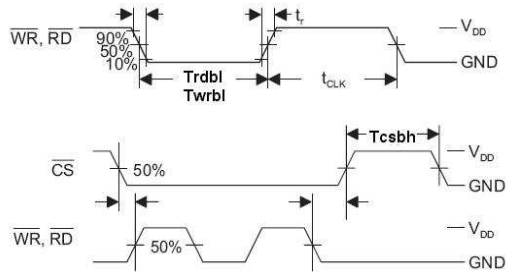
Pad No.	Pad Name	I/O	Function
1	CSB	I	Chip selection input with pull high resistor When the CS is logic high, the data and command read from or written to the SL6408 are disabled. The serial interface circuit is also reset. But if CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the SL6408 are all enabled.
2	RDB	I	READ clock input with pull high resistor Data in the RAM of the SL6408 are clocked out on the falling edge of the RD signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	WRB	I	WRITE clock input with pull high resistor Data on the DATA line are latched into the SL6408 on the rising edge of the WR signal.
4	DATA	I/O	Serial data input/output with pull high resistor
5	VSS	-	Negative power supply, ground
6	XIN_INDR	I	Use EL_EN pin to switch this pin as XIN or EL_R. EL_EN=1(EL_R), =0(XIN). Connect a resistor in series to VSS to adjust EL charging frequency.
7	XOUT_ELRL	I/O	Use EL_EN pin to switch this pin as XOUT or IND_R. EL_EN=1(IND_R), =0(XOUT). Connect a resistor in series to VSS to adjust EL discharging frequency.
8	VDD	-	Positive power supply
9	VLCD	I	LCD power input
10	IRQB	O	Time base or WDT overflow flag, NMOS open drain output
11,12	BZ, BZB	O	2KHz or 4KHz tone frequency output pair.
17~31	COM0~COM7	O	LCD common outputs
34~100	SEG0~SEG63	O	LCD segment outputs

## ● DC Character

Ta=25°C

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit.
		VDD	Conditions				
<b>ISTDB5</b>	Standby Current	5V	No load Power down mode		20		μA
<b>ISTDB3</b>	Standby Current	3V	No load Power down mode		10		μA
<b>IOP5</b>	Operation current	5V	No load, internal RC oscillator on		330		μA
<b>IOP3</b>	Operation current	3V	No load, internal RC oscillator on		200		μA
<b>Io1_5</b>	LCD Common Sink Current	5V	VOL=0V and short to 0.5V			2.4	mA
<b>Io2_5</b>	LCD Common Source Current	5V	VOH=5V and short to 4.5V			-0.5	mA
<b>Io3_5</b>	LCD Segment Sink Current	5V	VOL=0V and short to 0.5V			2.6	mA
<b>Io4_5</b>	LCD Segment Source Current	5V	VOH=5V and short to 4.5V			-0.6	mA
<b>Io5_5</b>	IND_BZ, EL_BZB Sink Current	5V	VOL=0V and short to 0.5V		21		mA
<b>Io6_5</b>	IND_BZ, EL_BZB Source Current	5V	VOH=5V and short to 4.5V		-5		mA
<b>Io1_3</b>	LCD Common Sink Current	3V	VOL=0V and short to 0.3V			1.0	mA
<b>Io2_3</b>	LCD Common Source Current	3V	VOH=5V and short to 2.7V			-0.27	mA
<b>Io3_3</b>	LCD Segment Sink Current	3V	VOL=0V and short to 0.3V			1.1	mA
<b>Io4_3</b>	LCD Segment Source Current	3V	VOH=5V and short to 2.7V			-0.26	mA
<b>Io5_3</b>	IND_BZ, EL_BZB Sink Current	3V	VOL=0V and short to 0.3V		8		mA
<b>Io6_3</b>	IND_BZ, EL_BZB Source Current	3V	VOH=5V and short to 2.7V		-3		mA

## ● AC Character

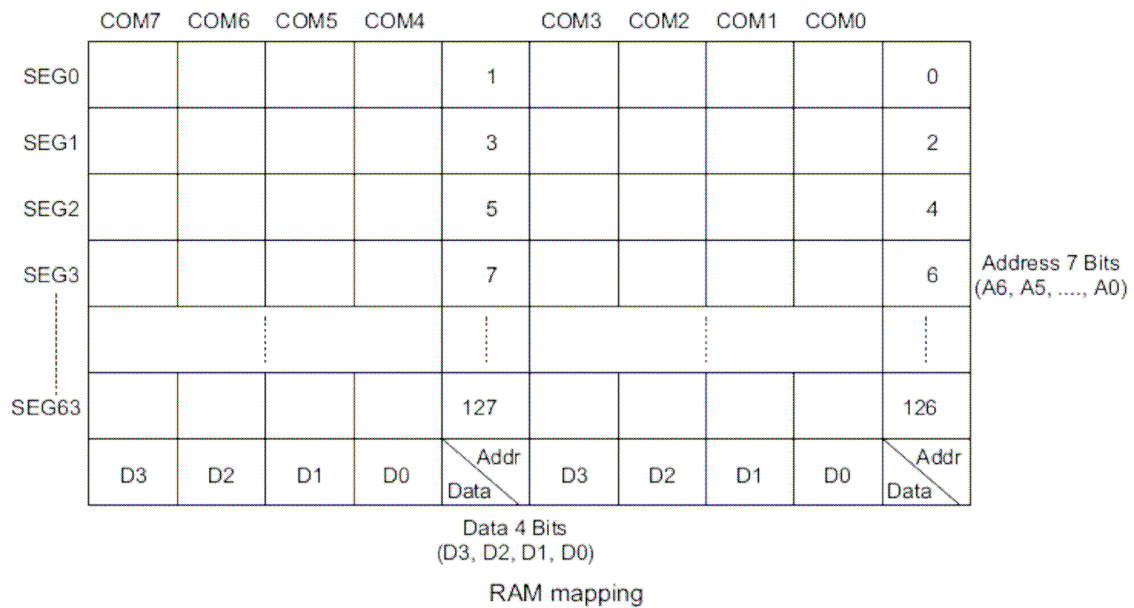


Symbol	Parameter	VDD	Min	Typ.	Max	Unit.
<b>F<sub>int3</sub></b>	Internal RC oscillator	3V		256		KHz
<b>F<sub>int5</sub></b>	Internal RC oscillator	5V		256		KHz
<b>F<sub>ext5</sub></b>	External input clock	5V			150	KHz
<b>T<sub>rdbl3</sub></b>	Minimum read low pulse	3V	350			ns
<b>T<sub>rdbl5</sub></b>	Minimum read low pulse	5V	350			ns
<b>T<sub>wrbl3</sub></b>	Minimum write low pulse	3V	350			ns
<b>T<sub>wrbl5</sub></b>	Minimum write low pulse	5V	350			ns
<b>T<sub>csbh5</sub></b>	Minimum CSB high pulse	5V	50			ns

## ● Functional Description

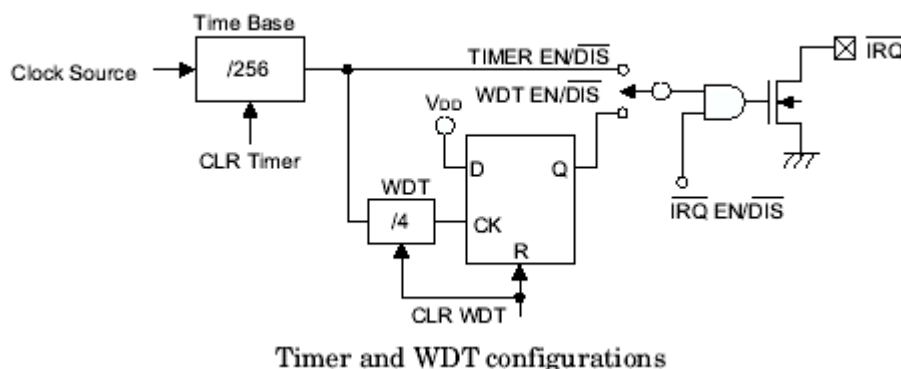
### Display Memory RAM

The static display RAM is organized into 96x4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.



### Time Base and Watchdog Timer (WDT)

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and IRQ EN/DIS are independent from each other. Once the WDT time-out occurs, the IRQ pin will remain at logic low level until the CLR WDT or the IRQ DIS command is issued. If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.



## Tone Output

A simple tone generator is implemented in the SL6408. The tone generator can output a pair of differential driving signals on the BZ and BZB pins, which are used to generate a single tone.

When "TONE OFF" condition, pin "BZ" is HI ,and pin "BZB" is LOW.

Suggest the buzzer using "PIEZO BUZZER" may obtain the better sound effect,

If use the "MAGNETIC BUZZER" to have two procedures:

1. Buzzer one pin link to the "VDD" another pin link to "BZ".
2. Buzzer one pin link to the "VSS" another pin link to "BZB".

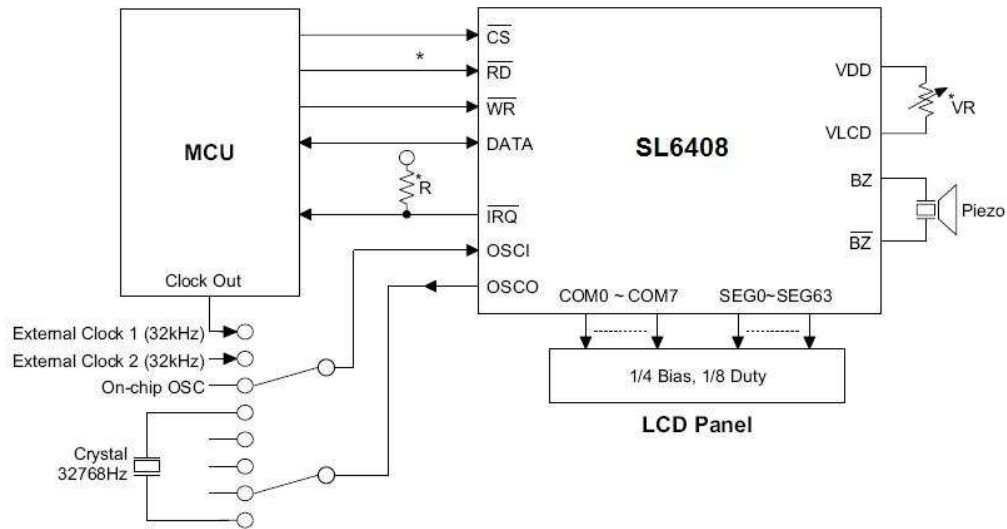
## Command Format

The SL6408 can be configured by the software. There are two mode commands to configure the SL6408 resource and to transfer the LCD display data.

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in a non-successive command or a non-successive address data mode, the CS pin should be set to "1" and the previous operation mode will be reset also. The CS pin returns to "0", a new operation mode ID should be issued first.

## ● Application Circuit



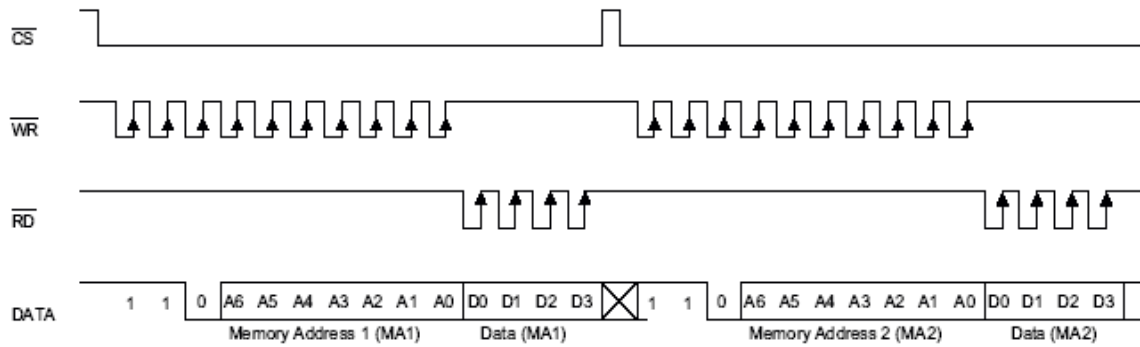
Host controller with a SL6408 display system

Note: The connection of IRQ and RD pin can be selected depending on the requirement of the Micro-C. The voltage applied to VLCD pin must be lower than VDD. Adjust VR to fit LCD display, at VDD=5V, VLCD=4V, VR about 20k. Adjust R (external pull-high resistance) to fit user's time base clock.

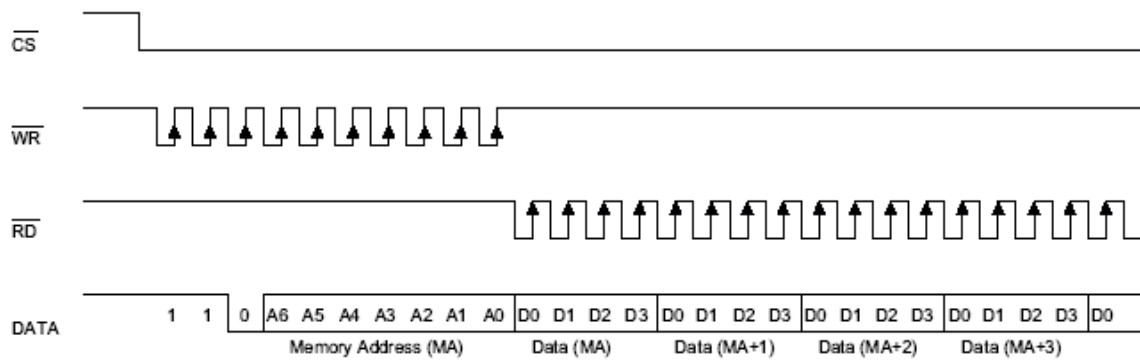


## ● Timing Diagram

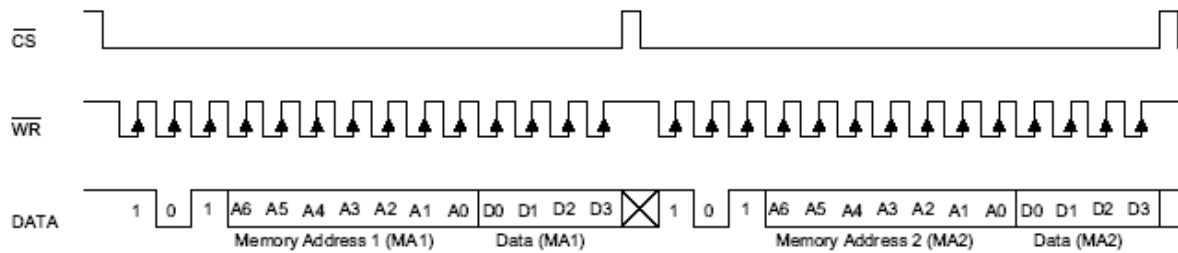
READ mode (command code : 1 1 0)



READ mode (successive address reading)



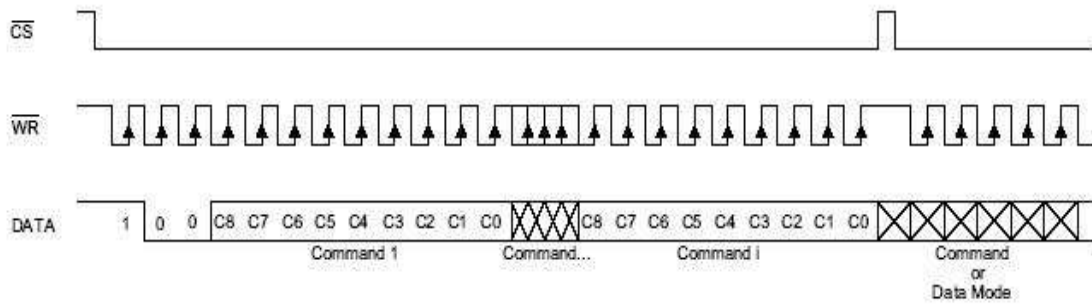
**WRITE mode (command code : 1 0 1)**



**WRITE mode (successive address writing)**



**Command mode (command code : 1 0 0)**



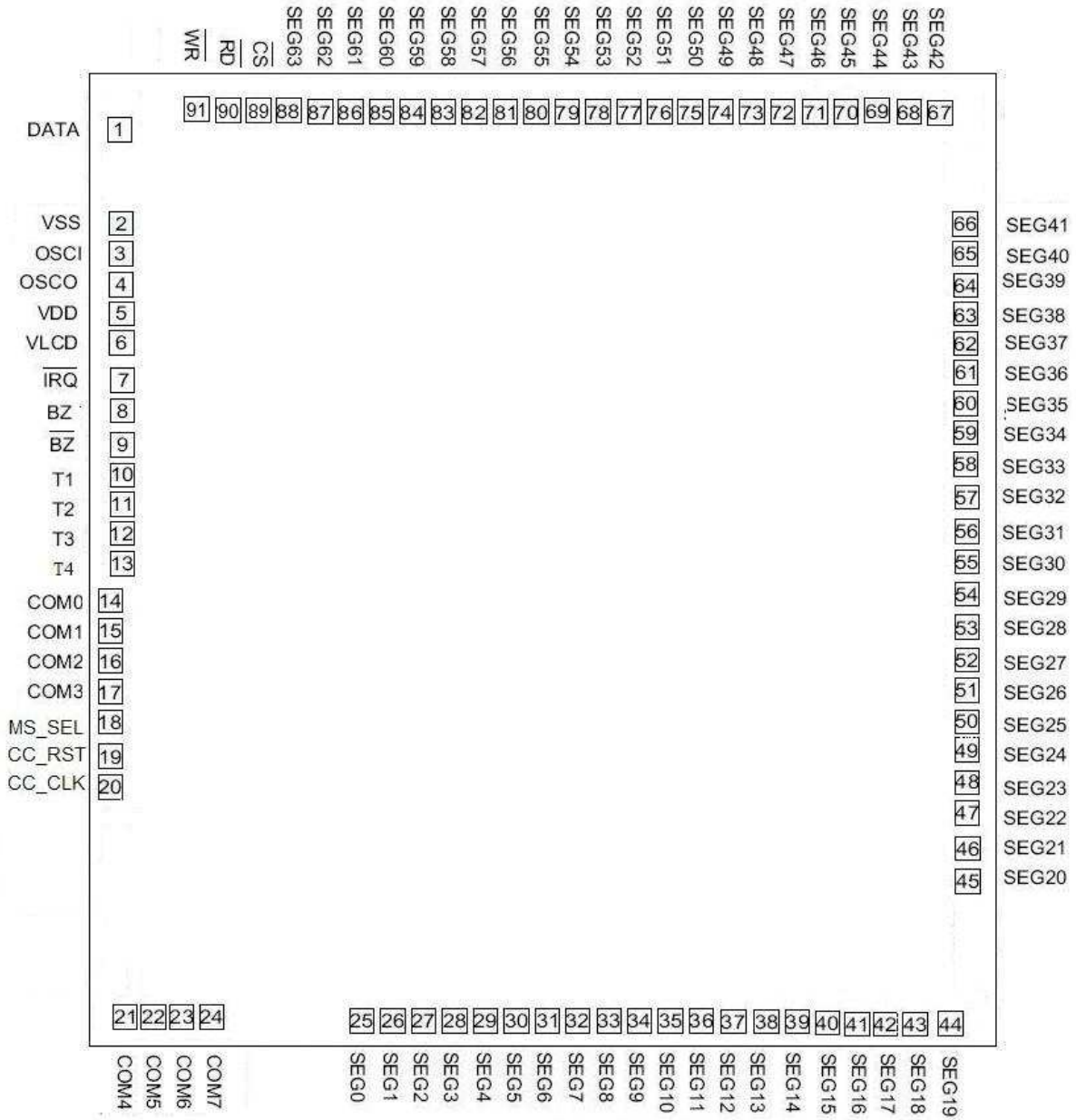
## ● Command Index

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A6A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	1 0 0	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	1 0 0	0000-1101-X	C	Clear the contents of time base generator	
CLR WDT	1 0 0	0000-1111-X	C	Clear the contents of WDT stage	
RC 32K	1 0 0	0001-10XX-X	C	System clock source, on chip RC oscillator	Yes
EXT 32K	1 0 0	0001-11XX-X	C	System clock source, external clock source	
TONE 4K	1 0 0	010X-XXXX-X	C	Tone frequency, 4KHz	
TONE 2K	1 0 0	011X-XXXX-X	C	Tone frequency, 2KHz	
IRQ DIS	1 0 0	100X-0XXX-X	C	Disable IRQ output	Yes
IRQ EN	1 0 0	100X-1XXX-X	C	Enable IRQ output	
F1	1 0 0	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	1 0 0	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	1 0 0	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	1 0 0	101X-X011-X	C	Time base/WDT clock Output: 8Hz The WDT time-out flag after: 1/2 s	
F16	1 0 0	101X-X100-X	C	Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4 s	
F32	1 0 0	101X-X101-X	C	Time base/WDT clock output: 32Hz The WDT time-out flag after: 1/8 s	
F64	1 0 0	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16 s	
F128	1 0 0	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32 s	Yes

Note: X: Don't care  
A6~A0: RAM addresses  
D3~D0: RAM data  
D/C: Data/command mode  
Def.: Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base or WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SL6408 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SL6408.

## ● Pin Assignment



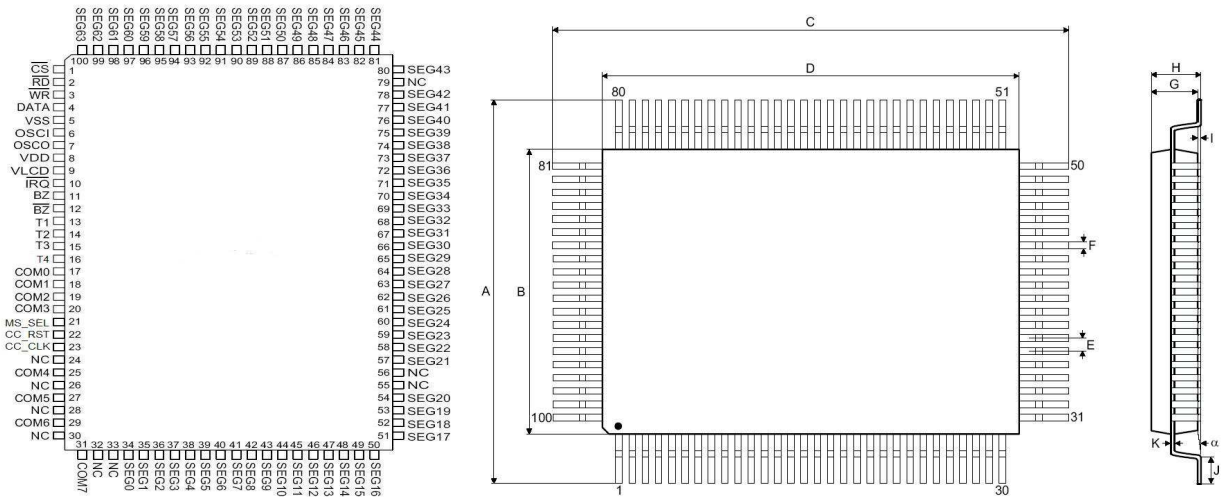
The IC substrate should be connected to VDD in the PCB layout artwork.

## ● Pad Coordinates

No.	Pin Name	X	Y	No.	Pin Name	X	Y	No.	Pin Name	X	Y
1	DATA	123.86	3077.14	32	SEG[7]	2148.41	81.51	63	SEG[38]	3657.5	2662.44
2	VSS	123.86	2866.71	33	SEG[8]	2267.87	81.51	64	SEG[39]	3657.5	2783.77
3	XIN_INDR	123.86	2748.02	34	SEG[9]	2388.32	81.51	65	SEG[40]	3657.5	2904.11
4	XOUT_ELR	123.86	2626.8	35	SEG[10]	2510.53	81.51	66	SEG[41]	3657.5	3026.32
5	VDD	123.86	2506.35	36	SEG[11]	2629.99	81.51	67	SEG[42]	3271.29	3098.59
6	VLCD	123.86	2385.02	37	SEG[12]	2752.2	81.51	68	SEG[43]	3149.96	3098.59
7	IRQB	123.86	2263.8	38	SEG[13]	2872.65	81.51	69	SEG[44]	3027.75	3098.59
8	IND_BZ	123.86	2137.08	39	SEG[14]	2994.75	81.51	70	SEG[45]	2908.29	3098.59
9	EL_BZB	123.86	2015.86	40	SEG[15]	3115.2	81.51	71	SEG[46]	2786.08	3098.59
10	T1	123.86	1880.23	41	SEG[16]	3236.53	81.51	72	SEG[47]	2665.74	3098.59
11	T2	123.86	1757.14	42	SEG[17]	3355.99	81.51	73	SEG[48]	2544.41	3098.59
12	T3	123.86	1637.68	43	SEG[18]	3478.2	81.51	74	SEG[49]	2423.08	3098.59
13	T4	123.86	1517.23	44	SEG[19]	3599.53	81.51	75	SEG[50]	2302.74	3098.59
14	COM[0]	80.08	1357.62	45	SEG[20]	3657.5	484.44	76	SEG[51]	2181.41	3098.59
15	COM[1]	80.08	1236.29	46	SEG[21]	3657.5	604.89	77	SEG[52]	2060.96	3098.59
16	COM[2]	80.08	1115.07	47	SEG[22]	3657.5	726.11	78	SEG[53]	1939.74	3098.59
17	COM[3]	80.08	994.62	48	SEG[23]	3657.5	847.44	79	SEG[54]	1818.41	3098.59
18	MS_SEL	80.08	873.29	49	SEG[24]	3657.5	968.77	80	SEG[55]	1697.08	3098.59
19	CC_RST	80.08	752.95	50	SEG[25]	3657.5	1089.11	81	SEG[56]	1576.74	3098.59
20	CC_CLK	80.08	632.5	51	SEG[26]	3657.5	1210.44	82	SEG[57]	1455.41	3098.59
21	COM[4]	159.61	81.51	52	SEG[27]	3657.5	1331.77	83	SEG[58]	1334.08	3098.59
22	COM[5]	279.95	81.51	53	SEG[28]	3657.5	1452.11	84	SEG[59]	1214.62	3098.59
23	COM[6]	401.28	81.51	54	SEG[29]	3657.5	1573.44	85	SEG[60]	1092.41	3098.59
24	COM[7]	522.17	81.51	55	SEG[30]	3657.5	1694.77	86	SEG[61]	971.96	3098.59
25	SEG[0]	1299.87	81.51	56	SEG[31]	3657.5	1815.11	87	SEG[62]	849.86	3098.59
26	SEG[1]	1420.21	81.51	57	SEG[32]	3657.5	1936.44	88	SEG[63]	729.41	3098.59
27	SEG[2]	1542.42	81.51	58	SEG[33]	3657.5	2057.77	89	CSB	592.02	3102.11
28	SEG[3]	1663.75	81.51	59	SEG[34]	3657.5	2177.23	90	RDB	471.68	3102.11
29	SEG[4]	1785.41	81.51	60	SEG[35]	3657.5	2299.44	91	WRB	351.23	3102.11
30	SEG[5]	1903.99	81.51	61	SEG[36]	3657.5	2420.77				
31	SEG[6]	2025.32	81.51	62	SEG[37]	3657.5	2541.99				

● Package

QFP100



A	B	C	D	E	F	G	H	I	J	K	$\alpha$	Unit
18.5~19.2	13.9~14.1	24.5~25.2	19.9~20.1	0.65	0.3	2.5~3.1	3.4	0.1	1~1.40	0.10~0.20	0°~7°	mm

**● History**

Date	Name	Version	Comment
2008/2/27	Ken	1.0	Initial
2008/3/18	Ken	1.1	modify DC Character
2008/5/29	Ken	1.2	modify Buzzer account and DC Character
2008/7/9	Ken	1.3	modify Pad Coordinates