SL4816 Data sheet description Ver3.7

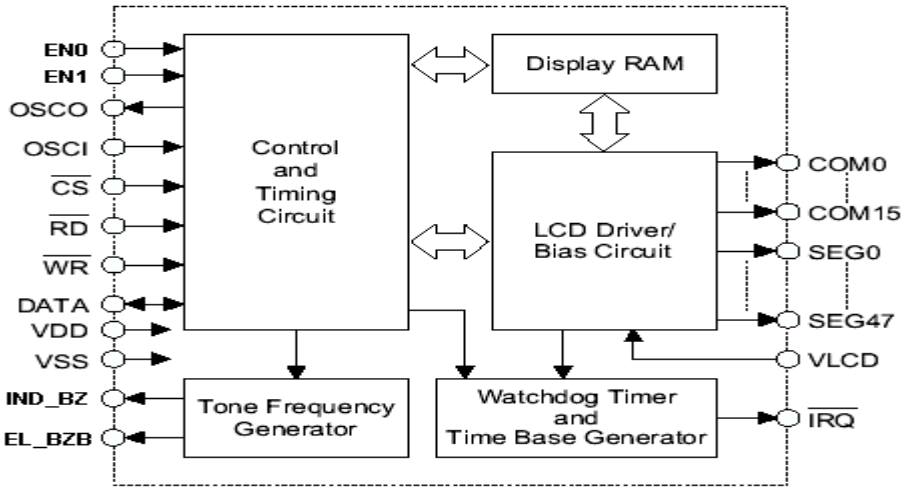
Features

- Operating voltage: 2.4V~5.2V
- Built-in RC oscillator
- External 32.768kHz crystal or 32kHz frequency source input
- 1/5 bias, 1/16 duty, frame frequency is 64Hz
- Max.48x16 patterns, 16commons, 48segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base/WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selection buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Cascade application
- EL application (Only available by internal RC oscillator)

General Description

SL4816 is a peripheral device specially designed for I/O type Micro-C used to expand the display capability. The display segments of the device are 768 patterns (48x16). It also supports serial interface, buzzer sound, watchdog Timer or time base timer functions. The SL4816 is a memory mapping and multi-function LCD controller. The software configuration feature of the SL4816 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the SL4816.

Block Diagram



Note: CSB: Chip selection
IND_BZ, EL_BZB: Tone outputs
WRB, RDB, DATA: Serial interface
COM0~COM15, SEG0~SEG47: LCD outputs
IRQB: Time base or WDT overflow output

● Pad Description

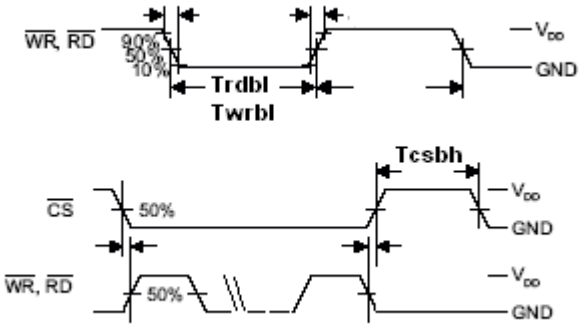
Pad No.	Pad Name	I/O	Function
81	CSB	I	Chip selection input with pull high resistor When the CS is logic high, the data and command read from or written to the SL3208 are disabled. The serial interface circuit is also reset. But if CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the SL3208 are all enabled.
82	RDB	I	READ clock input with pull-high resistor. Data in the RAM of the SL4816 are clocked out on the rising edge of the RD signal. The clocked out data will appear on the data line. The host controller can use the next falling edge to latch the clocked out data.
1	WRB	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the SL4816 on the rising edge of the WR signal.
2	DATA	I/O	Serial data input/output with pull-high resistor
3	EN0	I	EL/Buzzer function selection input.
4	EN1	I	EL/Buzzer function selection input.
5	VSS	-	Negative power supply, ground
6	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
7	OSCO	O	
8	VLCD	I	LCD power input
9	VDD	-	Positive power supply
10	IRQB	O	Time base or WDT overflow flag, NMOS open drain output
11~12	IND_BZ,EL_BZB	O	2KHz or 4KHz tone frequency output pair, EL function output
13~28	COM0~COM15	O	LCD common outputs
29~80	SEG47~SEG0	O	LCD segment outputs

● DC Characteristic

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit.
		VDD	Conditions				
I_{STDB5}	Standby Current	5V	No load Power down mode		20	40	uA
I_{STDB3}	Standby Current	3V	No load Power down mode		3	6	uA
I_{OP5}	Operation current	5V	No load, internal RC oscillator on		150	-	uA
I_{OP3}	Operation current	3V	No load, internal RC oscillator on		58	-	uA
I_{OLC}	LCD Common Sink Current	5V	VOL=0V and short to 5V		2.22		mA
I_{OHC}	LCD Common Source Current	5V	VOH=5V and short to 0V		-3.58		mA
I_{OLS}	LCD Segment Sink Current	5V	VOL=0V and short to 5V		3.76		mA
I_{OHS}	LCD Segment Source Current	5V	VOH=5V and short to 0V		-2.28		mA
V_{IH5}	Input high level (CSB, WRB, RDB, DATA)	5V		1.5	2		V
V_{IL5}	Input low level (CSB, WRB, RDB, DATA)	5V			2	2.5	V
V_{IH3}	Input high level (CSB, WRB, RDB, DATA)	3V			1.3	2.6	V
V_{IL3}	Input low level (CSB, WRB, RDB, DATA)	3V		1.0	1.3		V

● AC Character

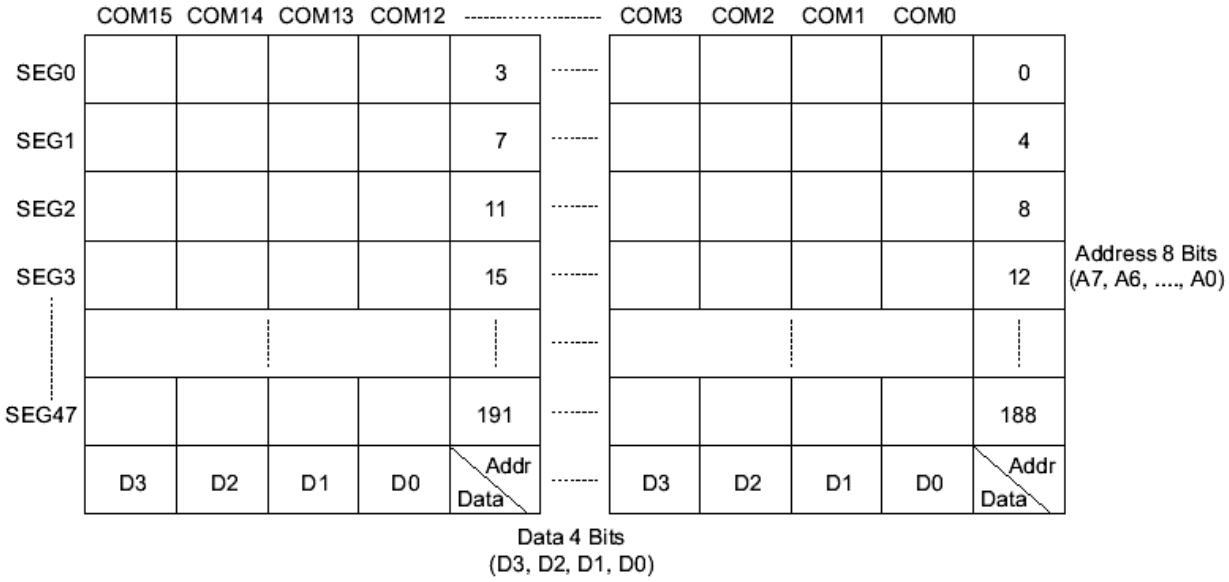


Symbol	Parameter	Vdd	Min	Typ.	Max	Unit.
F_{int3}	Internal RC oscillator	3V		176		KHz
F_{int5}	Internal RC oscillator	5V		314		KHz
F_{ext5}	External input clock	5V			300	KHz
T_{rdbl3}	Minimum read low pulse	3V	350			ns
T_{rdbl5}	Minimum read low pulse	5V	350			ns
T_{wrbl3}	Minimum write low pulse	3V	350			ns
T_{wrbl5}	Minimum write low pulse	5V	350			ns
T_{csbh5}	Minimum CSB high pulse	5V	50			ns

● Functional Description

Display Memory RAM

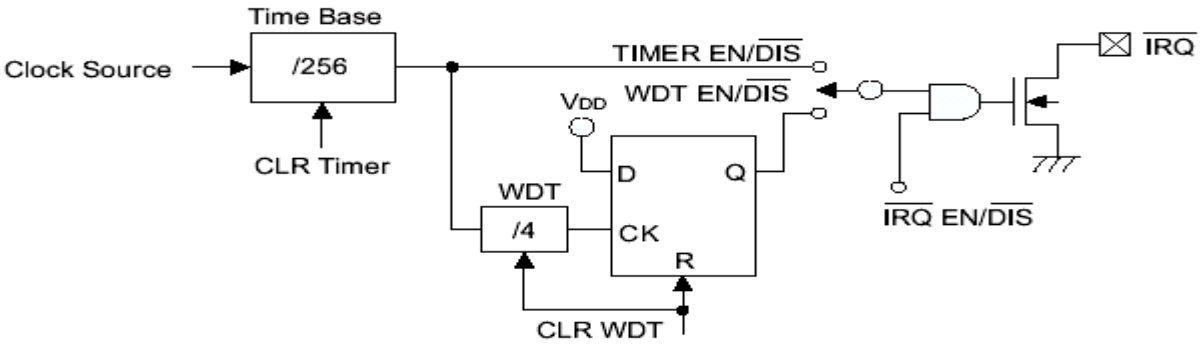
The static display RAM is organized into 192x4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.



RAM mapping

Time Base and Watchdog Timer (WDT)

The time base generator and WDT share the same divided (/256) counter. TIMERDIS/EN/CLR, WDT DIS/EN/CLR and IRQ EN/DIS are independent from each other. Once the WDT time-out occurs, the IRQ pin will remain at logic low level until the CLR WDT or the IRQ DIS command is issued. If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.



Tone Output

A simple tone generator is implemented in the SL4816. The tone generator can output a pair of differential driving signals on the IND_BZ and EL_BZB, which are used to generate a single tone.

Command Format

The SL4816 can be configured by set software. There are two mode commands to configure the SL4816 resource and to transfer the LCD display data.

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CS pin should be set to “1”, and the previous operation mode will be reset also. The CS pin returns to “0”, a new operation mode ID should be issued first.

EL Function

IND_BZ and EL_BZB are multi-functioned as part of EL application circuit by programming EN[1:0]. Four modes are available in this chip…

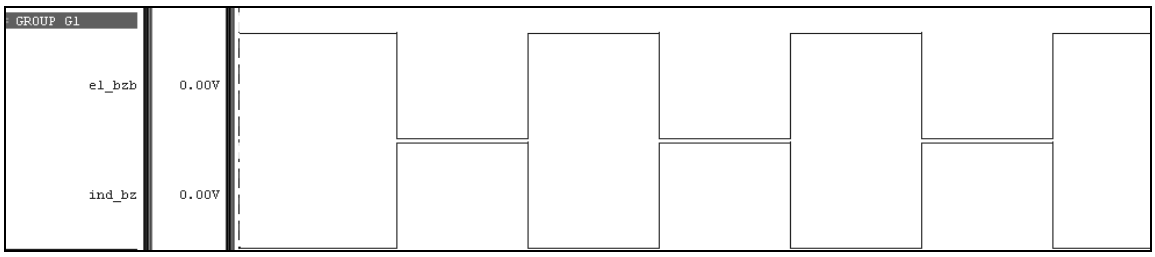
MODE	**EN[1:0]**	**Function**
MODE[0]	EN1: 0 EN0: 0	Function as Buzzer.
MODE[1]	EN1: 0 EN0: 1	Before issuing TONE OFF command, EL frequency output is determined by two commands, that is …“**TONE 2K**” and “**TONE 4k**”. For TONE 2K, the EL output frequency will be 500Hz For TONE 4K, the EL output frequency will be 1KHz
MODE[2]	EN1: 1 EN0: 0	Continuous 500Hz EL frequency output
MODE[3]	EN1: 1 EN0: 1	Continuous 1KHz EL frequency output

Note : Only available by internal RC oscillator

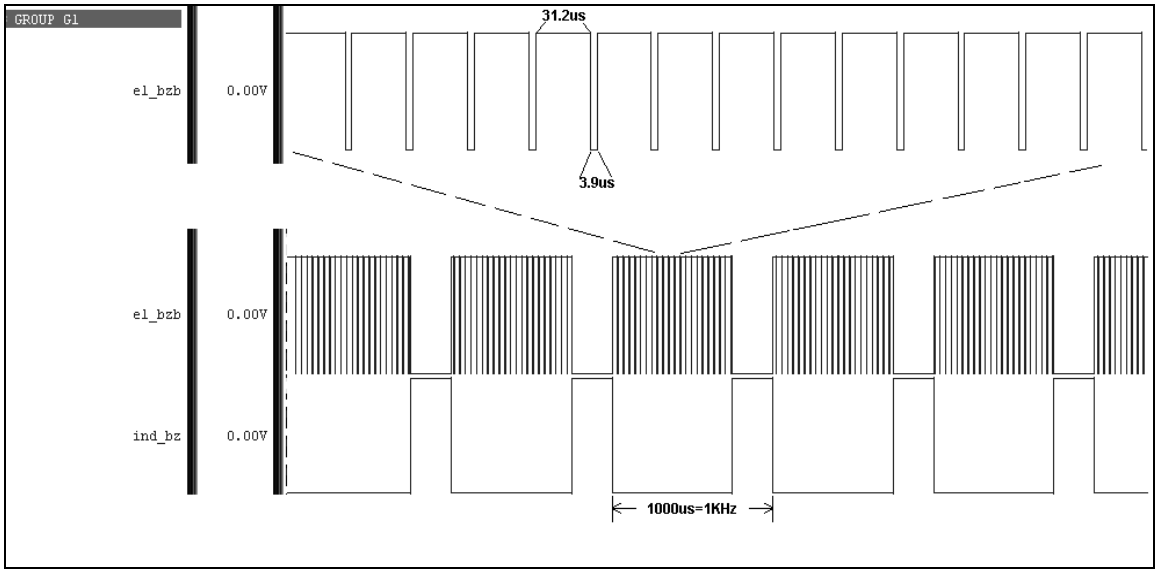
TONE 2K & TONE 4K only set the tone frequency (change frequency), can not active TONE output. It must use TONE ON instruction to let TONE output.

After power on, default is TONE 2K. TONE ON will cause TONE 2K frequency output. If you want the first output is TONE 4K, you can set TONE 4K before TONE ON instruction.

Buzzer waveform at (Mode 0):

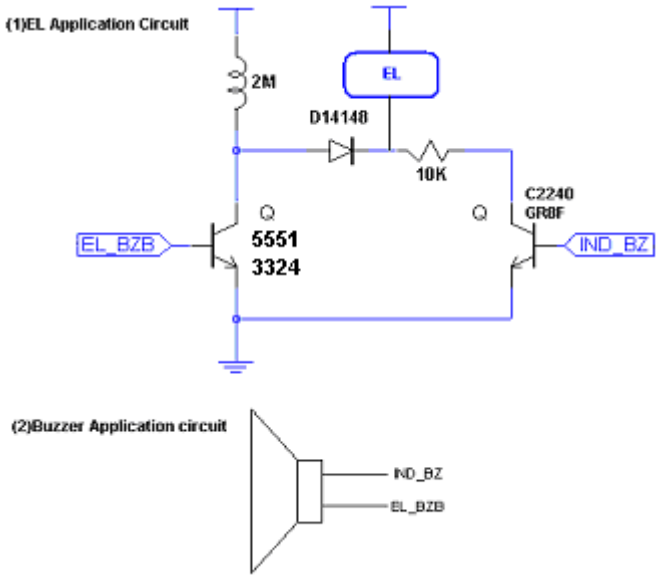


1KHz EL frequency output waveform at (Mode 1, 2 and 3):

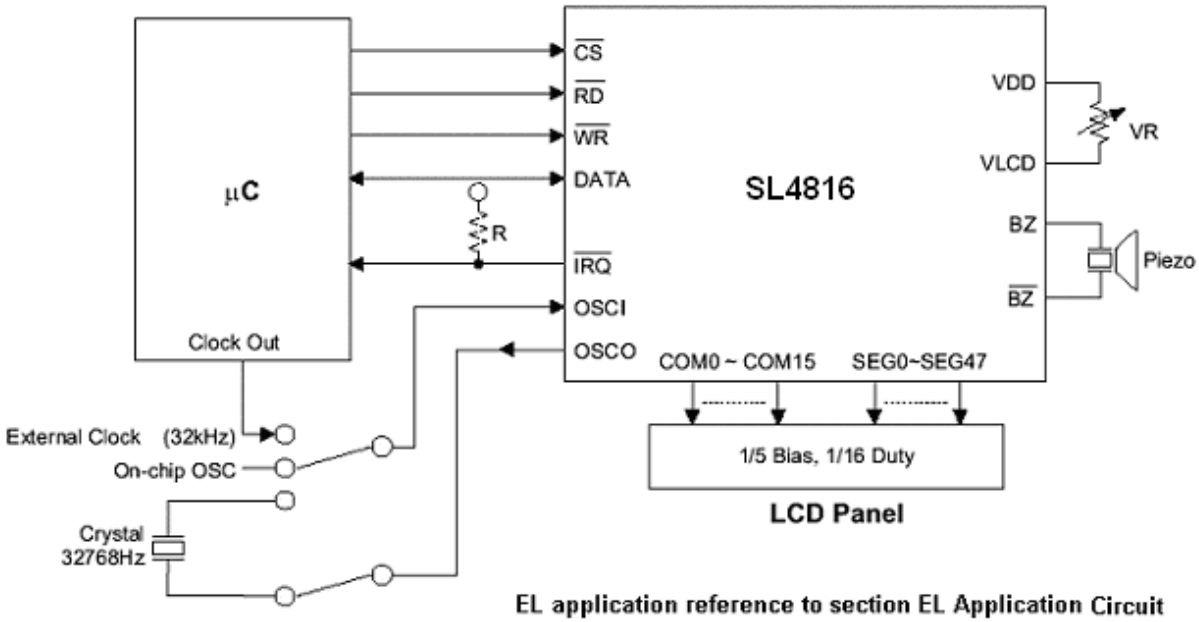


During charge period, the voltage at anode of diode (DN4148) is about 100V.

EL Application Circuit



● Application Circuit



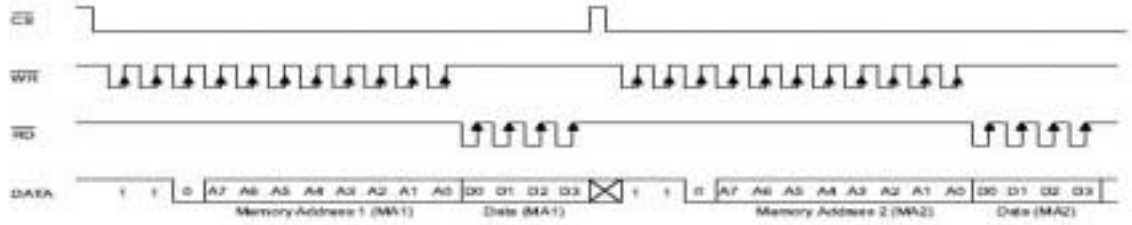
Host controller with a SL4816 display system

Note:

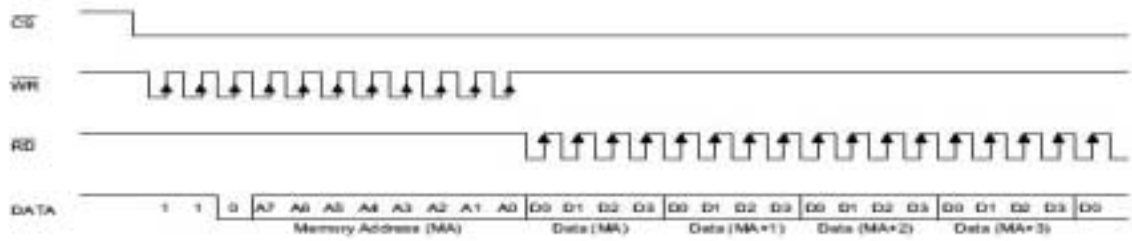
The connection of IRQ and RD pin can be selected depending on the requirement of the microprocessor. The voltage applied to V_{LCD} pin must be lower than V_{DD}. Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR about 20k . Adjust R (external pull-high resistance) to fit user s time base clock.

● Timing Diagram

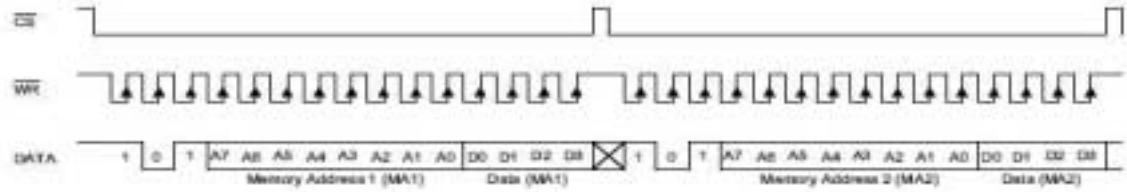
READ mode (command code : 1 1 0)



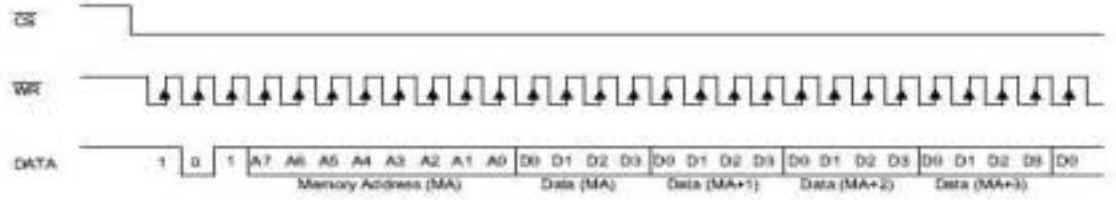
READ mode (successive address reading)



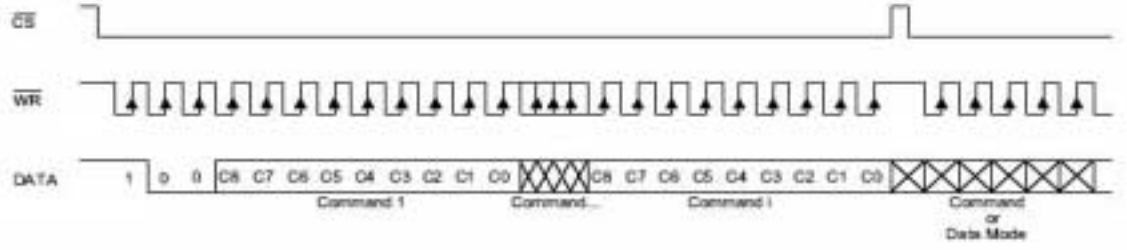
WRITE mode (command code : 1 0 1)



WRITE mode (successive address writing)



Command mode (command code : 1 0 0)



● Command Index

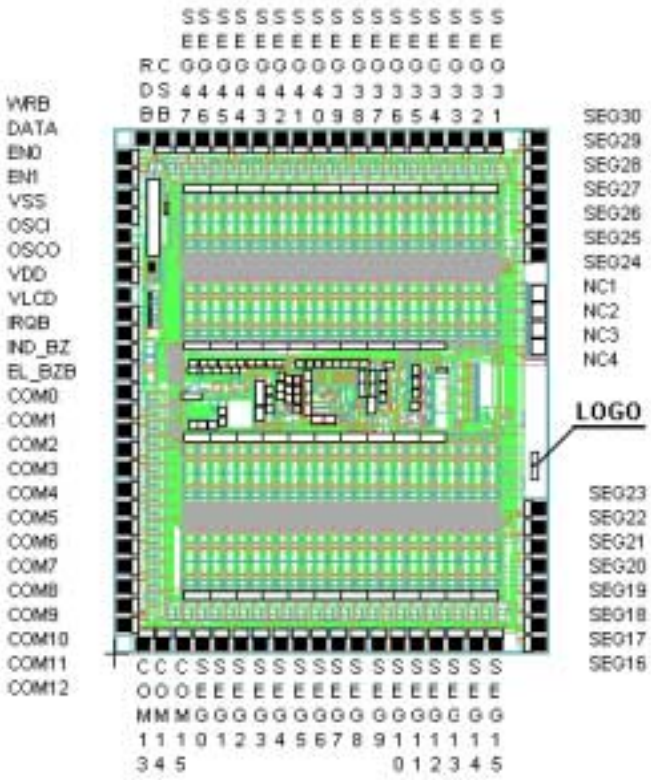
Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A7A6A5A4A3A2A1A0D0D1 D2D3	D	Read data from the RAM	
WRITE	1 0 1	A7A6A5A4A3A2A1A0D0D1 D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A7A6A5A4A3A2A1A0D0D1 D2D3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	1 0 0	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	1 0 0	0000-1101-X	C	Clear the contents of time base generator	
CLR WDT	1 0 0	0000-1111-X	C	Clear the contents of WDT stage	
RC 32K	1 0 0	0001-10XX-X	C	System clock source, on chip RC oscillator	Yes
EXT 32K	1 0 0	0001-11XX-X	C	System clock source, external clock source	
TONE 4K	1 0 0	010X-XXXX-X	C	Tone frequency, 4KHz	
TONE 2K	1 0 0	0110-XXXX-X	C	Tone frequency, 2KHz	
IRQ DIS	1 0 0	100X-0XXX-X	C	Disable IRQ output	Yes
IRQ EN	1 0 0	100X-1XXX-X	C	Enable IRQ output	
F1	1 0 0	101X-0000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	1 0 0	101X-0001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	1 0 0	101X-0010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	1 0 0	101X-0011-X	C	Time base/WDT clock Output: 8Hz The WDT time-out flag after: 1/2 s	
F16	1 0 0	101X-0100-X	C	Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4 s	
F32	1 0 0	101X-0101-X	C	Time base/WDT clock output: 32Hz The WDT time-out flag after: 1/8 s	

F64	1 0 0	101X-0110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16 s	
F128	1 0 0	101X-0111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32 s	Yes

Note: X: Don't care
A5~A0: RAM addresses
D3~D0: RAM data
D/C: Data/command mode
Def.: Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SL4816 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SL4816.

Pin Assignment



The IC substrate should be connected to VDD in the PCB layout artwork.

● Pad Coordinates

No.	Pin Name	X	Y	No.	Pin Name	X	Y
1	WRB	60.8	3260	45	SEG16	2777.6	60
2	DATA	60.8	3132.8	46	SEG17	2777.6	188
3	EN0	60.8	3004.8	47	SEG18	2777.6	316.8
4	EN1	60.8	2876	48	SEG19	2777.6	444.8
5	VSS	60.8	2747.2	49	SEG20	2777.6	571.2
6	OSCI	60.8	2620.8	50	SEG21	2777.6	700
7	OSCO	60.8	2492.8	51	SEG22	2777.6	827.2
8	VDD	60.8	2364	52	SEG23	2777.6	956.8
9	VLCD	60.8	2236	53	NC4	2777.6	2013.6
10	IRQB	60.8	2108.8	54	NC3	2777.6	2132
11	IND_BZ	60.8	1980.8	55	NC2	2777.6	2256
12	EL_BZB	60.8	1852	56	NC1	2777.6	2373.6
13	COM0	60.8	1724	57	SEG24	2777.6	2620.8
14	COM1	60.8	1596	58	SEG25	2777.6	2747.2
15	COM2	60.8	1468.8	59	SEG26	2777.6	2875.2
16	COM3	60.8	1340	60	SEG27	2777.6	3004
17	COM4	60.8	1212	61	SEG28	2777.6	3132.8
18	COM5	60.8	1084	62	SEG29	2777.6	3260
19	COM6	60.8	956	63	SEG30	2777.6	3387.2
20	COM7	60.8	828	64	SEG31	2492.8	3388
21	COM8	60.8	699.2	65	SEG32	2366.4	3388
22	COM9	60.8	572	66	SEG33	2238.4	3388
23	COM10	60.8	444.8	67	SEG34	2108.8	3388
24	COM11	60.8	315.2	68	SEG35	1981.6	3388
25	COM12	60.8	188	69	SEG36	1854.4	3388
26	COM13	189.6	60	70	SEG37	1726.4	3388
27	COM14	316.8	60	71	SEG38	1597.6	3388
28	COM15	444.8	60	72	SEG39	1469.6	3388
29	SEG0	573.6	60	73	SEG40	1342.4	3388
30	SEG1	702.4	60	74	SEG41	1213.6	3388
31	SEG2	828.8	60	75	SEG42	1085.6	3388
32	SEG3	956.8	60	76	SEG43	957.6	3388
33	SEG4	1085.6	60	77	SEG44	828.8	3388
34	SEG5	1214.4	60	78	SEG45	702.4	3388

35	SEG6	1340.8	60	79	SEG46	573.6	3388
36	SEG7	1469.6	60	80	SEG47	444.8	3388
37	SEG8	1597.6	60	81	CSB	316.8	3388
38	SEG9	1726.4	60	82	RDB	190.4	3388
39	SEG10	1854.4	60				
40	SEG11	1981.6	60				
41	SEG12	2109.6	60				
42	SEG13	2238.4	60				
43	SEG14	2366.4	60				
44	SEG15	2492.8	60		LOGO	2750.4	1236

- **History**

Date	Name	Version	Comment

2003/2/12	CC Kuo	1.0	Initial
2003/2/13	CC Kuo	1.1	
2003/2/26	CC Kuo	1.2	
2003/5/26	CC Kuo	2.0	
2003/6/11	CC Kuo	2.1	
2003/7/9	CC Kuo	2.2	Modified the DC spec. and Timing diagram
2003/7/10	CC Kuo	2.3	Modified the DC spec. add Vdd = 3v
2003/8/25	CC Kuo	2.4	Modified the DC spec. add Vdd = 3v
2003/9/05	CC Kuo	3.0	Create the SL4816
2003/9/20	CC Kuo	3.1	Add AC timing spec.
2004/2/24	CC Kuo	3.2	Modify the AC spec.
2004/4/27	CC Kuo	3.3	
2005/6/16	A.C.Lin	3.4	Timing diagram bug fixed.and modify the Operating voltage
2005/6/16	Rong	3.5	Modify command index
2005/9/6	Alan	3.6	Rmove EL_OFF and BZ_OFF ‘s delay 5 seconds
2005/10/3	A.C.Lin	3.7	Add Buzzer function