SL4808 Data sheet description Ver1.5

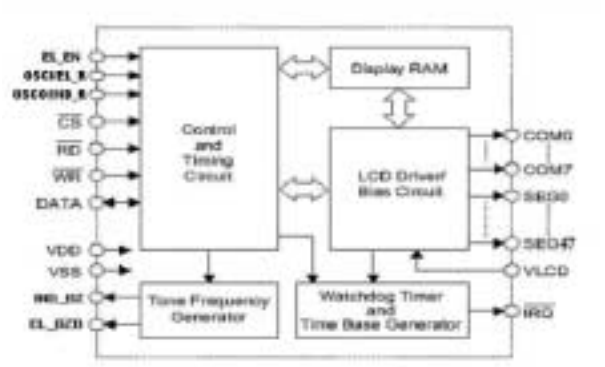
Features

- Operating voltage: 2.4V~5.2V
- Built-in RC oscillator
- External 32.768kHz crystal or 32kHz frequency source input
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 48x8 patterns, 8 commons, 48 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base/WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Cascade application
- EL application (The charging and discharging frequency of EL are adjusted by two external resistors.)

General Description

SL4808 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 384 patterns (48x8). It also supports serial interface, buzzer sound, watchdog timer or time base timer functions. The SL4808 is a memory mapping and multi-function LCD controller. The software configuration feature of SL4808 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the SL4808.

Block Diagram



Note: CSB: Chip selection
IND_BZ, EL_BZB: Tone outputs/EL application
WRB, RDB, DATA: Serial interface
COM0~COM7, SEG0~SEG47: LCD outputs
IRQB: Time base or WDT overflow output

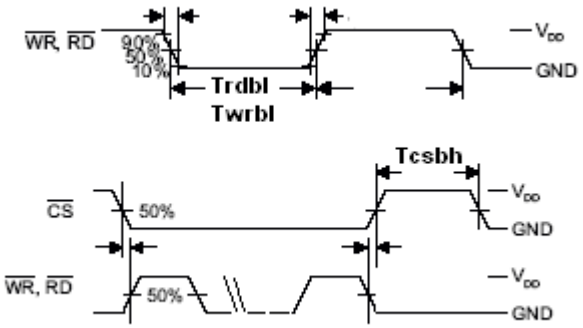
● Pad Description

Pad No.	Pad Name	I/O	Function
1	CSB	I	Chip selection input with pull high resistor When the CS is logic high, the data and command read from or written to the SL4808 are disabled. The serial interface circuit is also reset. But if CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the SL4808 are all enabled.
2	RDB	I	READ clock input with pull high resistor Data in the RAM of the SL4808 are clocked out on the falling edge of the RD signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	WRB	I	WRITE clock input with pull high resistor Data on the DATA line are latched into the SL4808 on the rising edge of the WR signal.
4	DATA	I/O	Serial data input/output with pull high resistor
5	EL_EN	I	EL/Buzzer function selection input. EL_EN=1 EL function, 0 Buzzer function
6	VSS	-	Negative power supply, ground
7	XIN_INDR	I	Use EL_EN pin to switch this pin as XIN or EL_R. EL_EN=1(EL_R), =0(XIN). Connect a resistor in series to VSS to adjust EL charging frequency.
8	XOUT_ELR	I/O	Use EL_EN pin to switch this pin as XOUT or IND_R. EL_EN=1(IND_R), =0 (XOUT). Connect a resistor in series to VSS to adjust EL discharging frequency.
9	VDD	-	Positive power supply
10	VLCD	I	LCD power input
11	IRQB	O	Time base or WDT overflow flag, NMOS open drain output
12,13	IND_BZ, EL_BZB	O	2KHz or 4KHz tone frequency output pair, EL function output.
14~21	COM0~COM7	O	LCD common outputs
22~69	SEG0~SEG47	O	LCD segment outputs

● DC Character

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit.
		VDD	Conditions				
I_{STDB5}	Standby Current	5V	No load Power down mode		5	10	μA
I_{STDB3}	Standby Current	3V	No load Power down mode		2	4	μA
I_{OP5}	Operation current	5V	No load, internal RC oscillator on		140		μA
I_{OP3}	Operation current	3V	No load, internal RC oscillator on		60		μA
$I_{o\_EL\_BZB}$	EL_BZB Sink Current	3V	VOL=0V and short to 0.8V		11.2		mA
I_{o1_5}	LCD Common Sink Current	5V	VOL=0V and short to 0.5V		200		uA
I_{o2_5}	LCD Common Source Current	5V	VOH=5V and short to 4.5V		-90		uA
I_{o3_5}	LCD Segment Sink Current	5V	VOL=0V and short to 0.5V		150		uA
I_{o4_5}	LCD Segment Source Current	5V	VOH=5V and short to 4.5V		40		uA
I_{o1_3}	LCD Common Sink Current	3V	VOL=0V and short to 0.3V		40		uA
I_{o2_3}	LCD Common Source Current	3V	VOH=5V and short to 2.7V		-30		uA
I_{o3_3}	LCD Segment Sink Current	3V	VOL=0V and short to 0.3V		30		uA
I_{o4_3}	LCD Segment Source Current	3V	VOH=5V and short to 2.7V		-13		uA

● AC Character

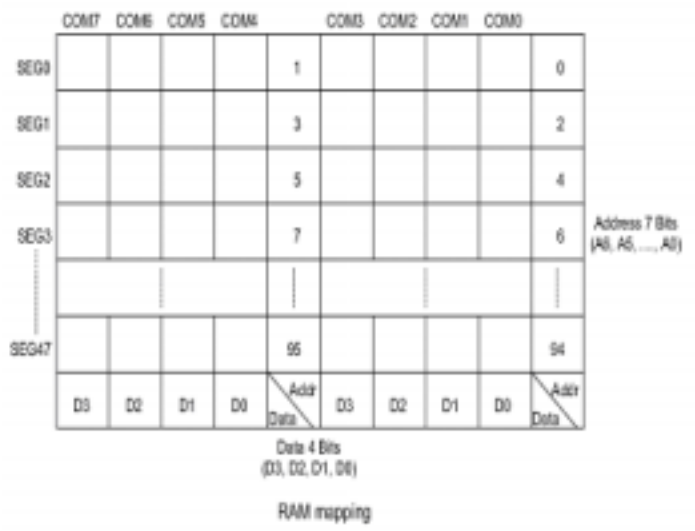


Symbol	Parameter	Vdd	Min	Typ.	Max	Unit.
F_{int3}	Internal RC oscillator	3V		226		KHz
F_{int5}	Internal RC oscillator	5V		430		KHz
F_{ext5}	External input clock	5V			150	KHz
T_{rdbl3}	Minimum read low pulse	3V	350			ns
T_{rdbl5}	Minimum read low pulse	5V	350			ns
T_{wrbl3}	Minimum write low pulse	3V	350			ns
T_{wrbl5}	Minimum write low pulse	5V	350			ns
T_{csbh5}	Minimum CSB high pulse	5V	50			ns

● Functional Description

Display Memory RAM

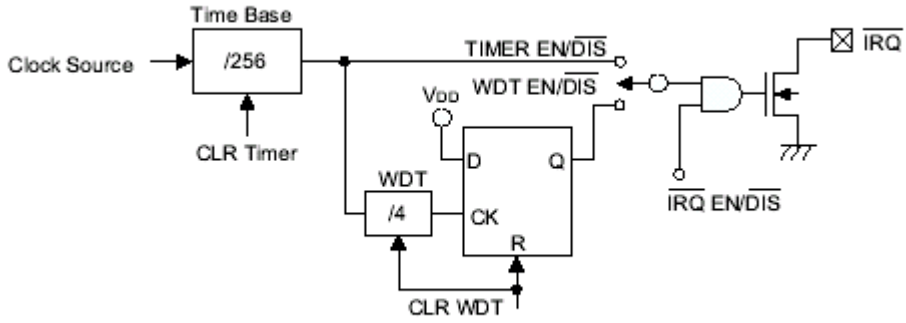
The static display RAM is organized into 96x4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.



RAM mapping

Time Base and Watchdog Timer (WDT)

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and IRQ EN/DIS are independent from each other. Once the WDT time-out occurs, the IRQ pin will remain at logic low level until the CLR WDT or the IRQ DIS command is issued. If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.



Timer and WDT configurations

Tone Output

A simple tone generator is implemented in the SL4808. The tone generator can output a pair of differential driving signals on the BZ and BZB pins, which are used to generate a single tone.

Command Format

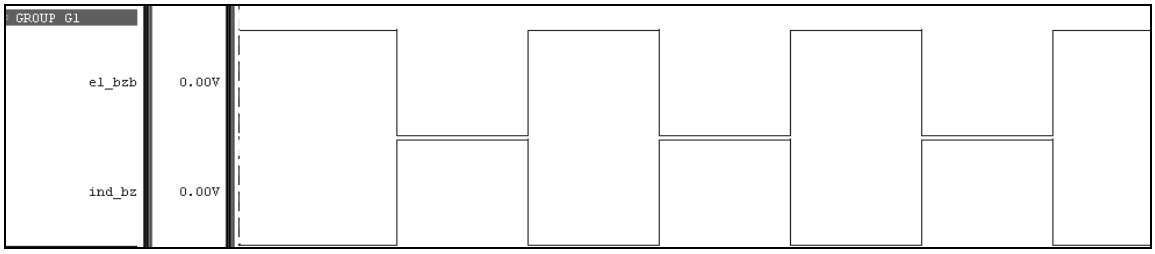
The SL4808 can be configured by the software. There are two mode commands to configure the SL4808 resource and to transfer the LCD display data.

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

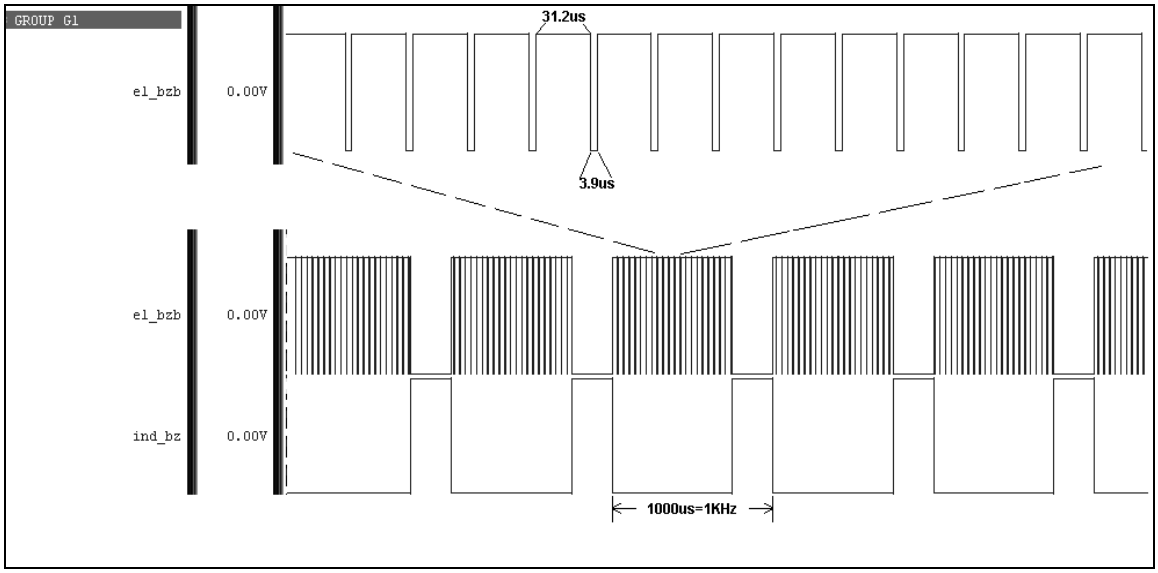
If successive commands have been issued, the command mode ID can be omitted. While the system is operating in a non-successive command or a non-successive address data mode, the CS pin should be set to "1" and the previous operation mode will be reset also. The CS pin returns to "0", a new operation mode ID should be issued first.

EL Function

EL_EN = 0 is Buzzer function, IND_BZ and EL_BZB pins output waveform as following, XIN_INDR and XOUT_ELR pins work as Crystal function.

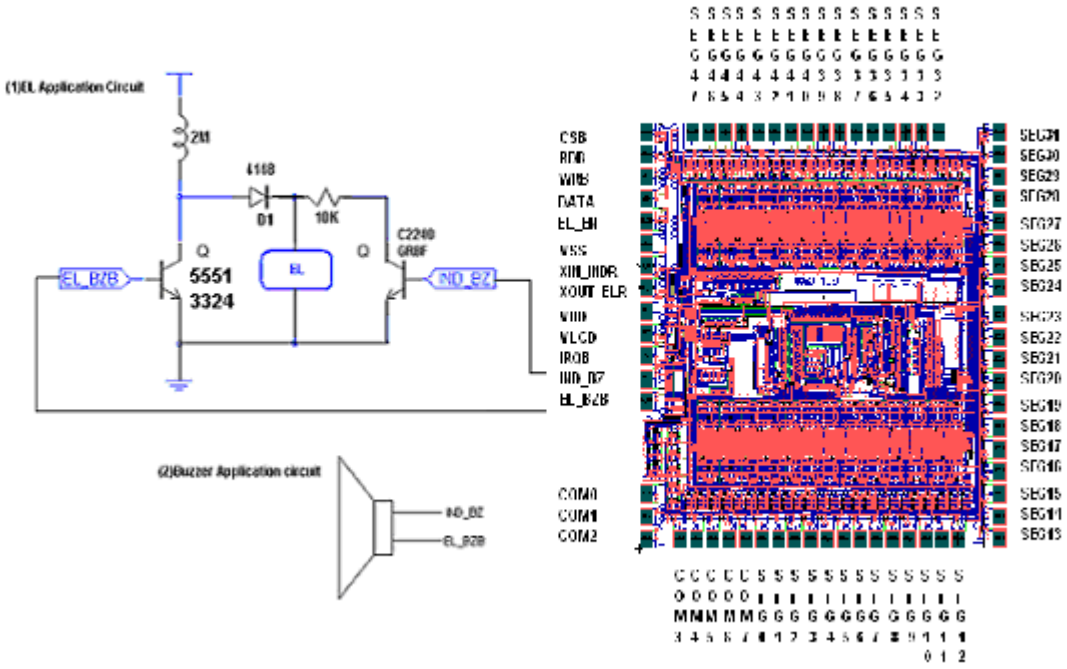


EL_EN = 1 is EL function, IND_BZ and EL_BZB pins output waveform as following, XIN_INDR and XOUT_ELR pins work as RC OSC.

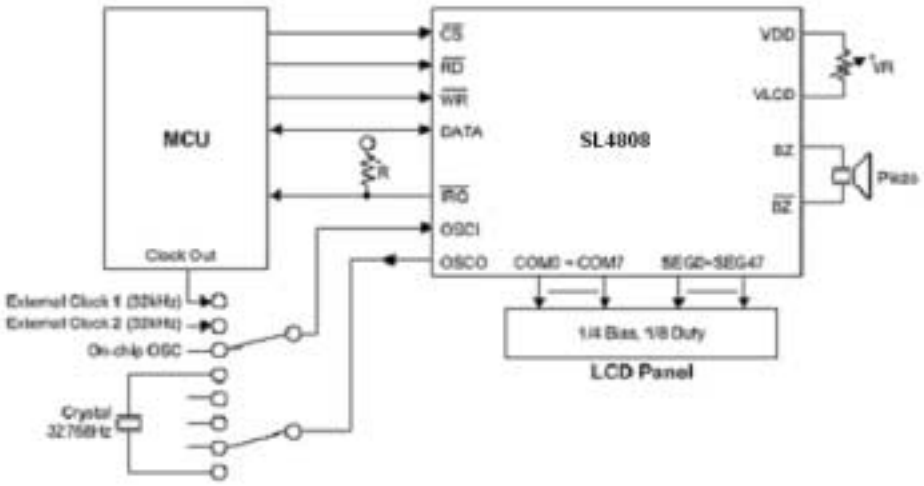


During charge period, the voltage at anode of single diode (D1N4148) is about 100V.

EL Application Circuit



● Application Circuit

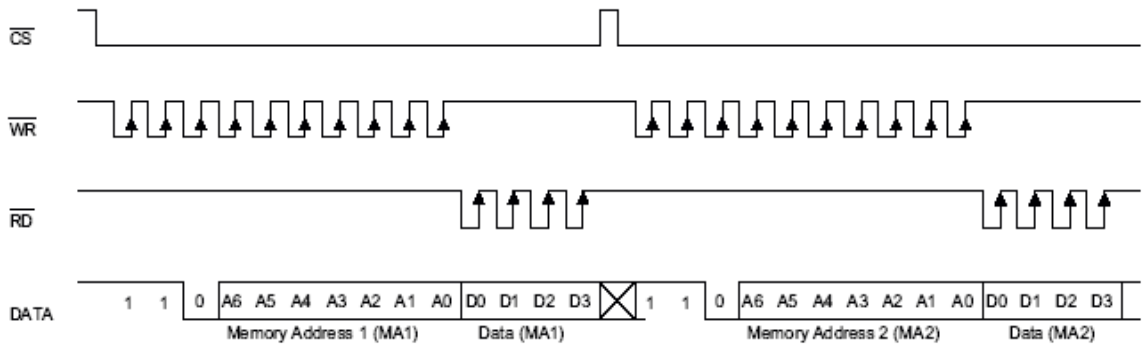


Host controller with a SL4808 display system

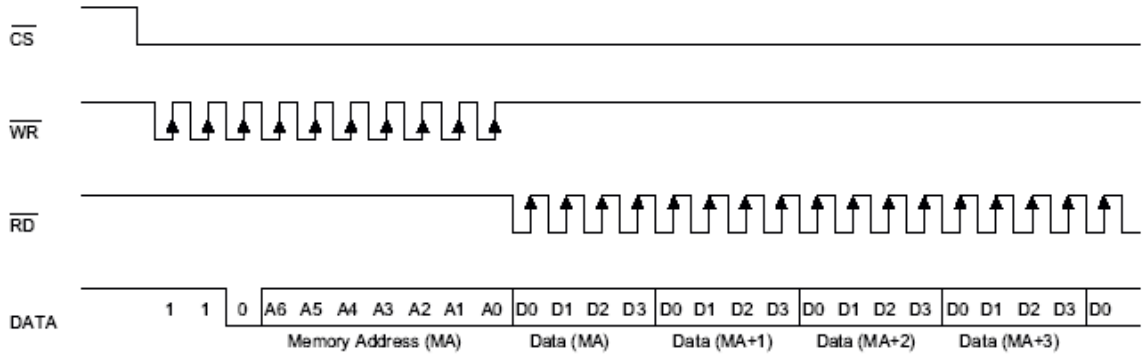
Note: The connection of IRQ and RD pin can be selected depending on the requirement of the Micro-C. The voltage applied to V_{LCD} pin must be lower than V_{DD}. Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR about 20k. Adjust R (external pull-high resistance) to fit user s time base clock.

● Timing Diagram

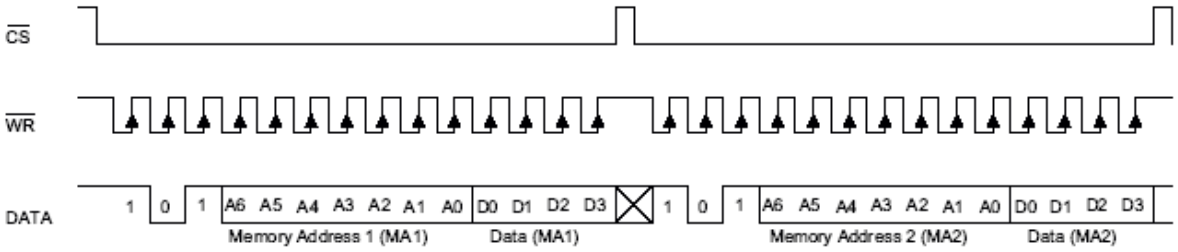
READ mode (command code : 1 1 0)



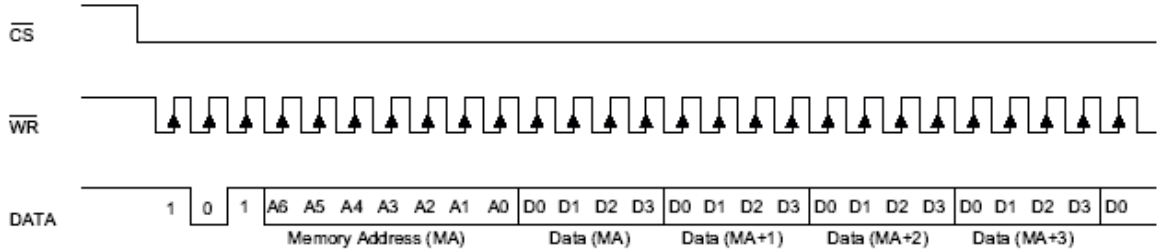
READ mdoe (successive address reading)

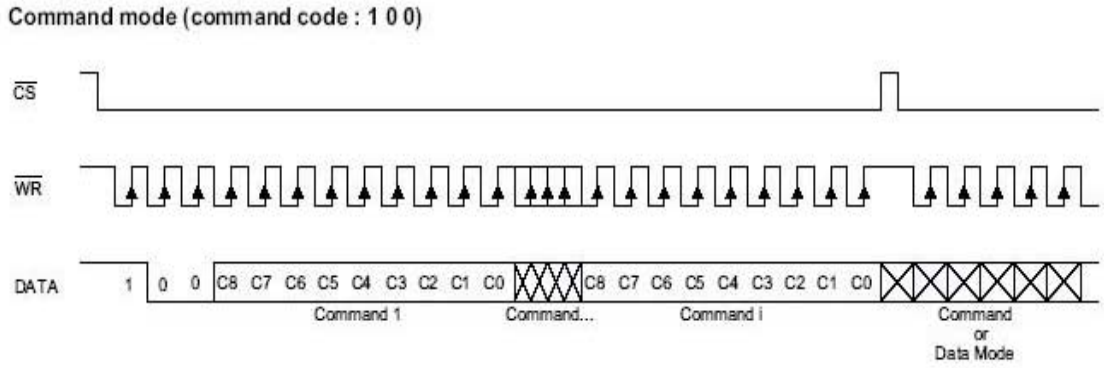


WRITE mode (command code : 1 0 1)



WRITE mode (successive address writing)





● Command Index

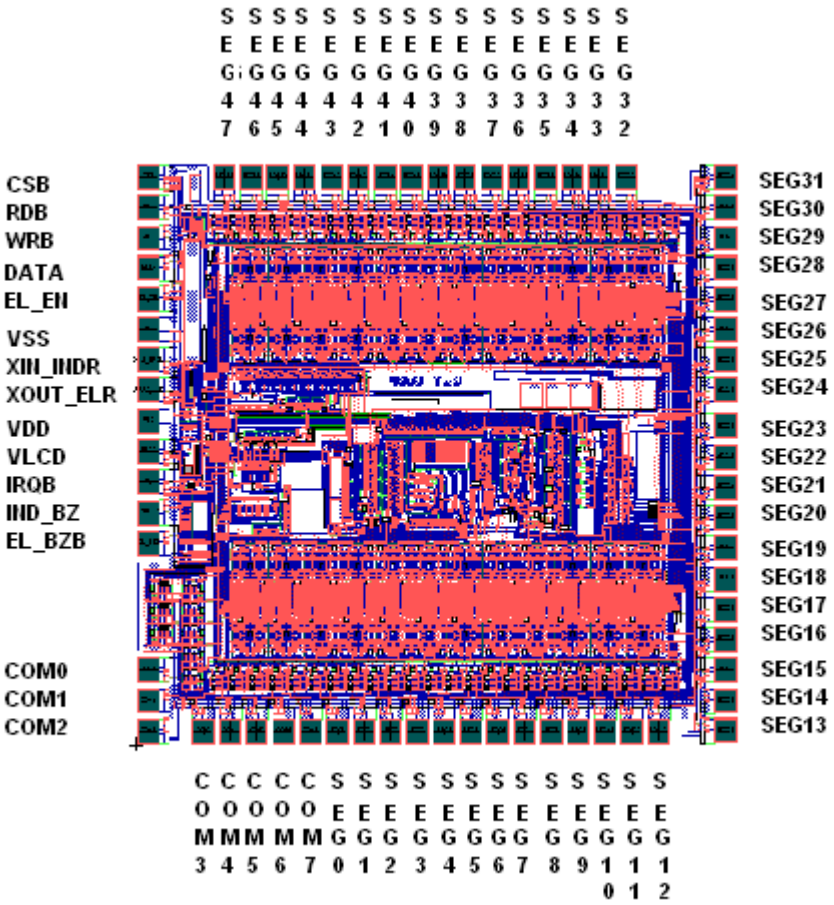
Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A6A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	1 0 0	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	1 0 0	0000-1101-X	C	Clear the contents of time base generator	
CLR WDT	1 0 0	0000-1111-X	C	Clear the contents of WDT stage	
RC 32K	1 0 0	0001-10XX-X	C	System clock source, on chip RC oscillator	Yes
EXT 32K	1 0 0	0001-11XX-X	C	System clock source, external clock source	
TONE 4K	1 0 0	010X-XXXX-X	C	Tone frequency, 4KHz	
TONE 2K	1 0 0	011X-XXXX-X	C	Tone frequency, 2KHz	
IRQ DIS	1 0 0	100X-0XXX-X	C	Disable IRQ output	Yes
IRQ EN	1 0 0	100X-1XXX-X	C	Enable IRQ output	
F1	1 0 0	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	1 0 0	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT	

				time-out flag after: 2s	
F4	1 0 0	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	1 0 0	101X-X011-X	C	Time base/WDT clock Output: 8Hz The WDT time-out flag after: 1/2 s	
F16	1 0 0	101X-X100-X	C	Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4 s	
F32	1 0 0	101X-X101-X	C	Time base/WDT clock output: 32Hz The WDT time-out flag after: 1/8 s	
F64	1 0 0	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16 s	
F128	1 0 0	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32 s	Yes

Note: X: Don't care
A6~A0: RAM addresses
D3~D0: RAM data
D/C: Data/command mode
Def.: Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base or WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SL4808 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SL4808.

Pin Assignment



The IC substrate should be connected to VDD in the PCB layout artwork.

● Pad Coordinates

No.	Pin Name	X	Y	No.	Pin Name	X	Y
1	CSB	60.8	2386	38	SEG16	2821.2	444.8
2	RDB	60.8	2258	39	SEG17	2821.2	572.8
3	WRB	60.8	2130	40	SEG18	2821.2	700.8
4	DATA	60.8	2002	41	SEG19	2821.2	828.8
5	EL_EN	60.8	1874	42	SEG20	2821.2	956.8
6	VSS	60.8	1746	43	SEG21	2821.2	1084.8
7	XIN_INDR	60.8	1618	44	SEG22	2821.2	1212.8
8	XOUT_ELR	60.8	1490	45	SEG23	2821.2	1340.8
9	VDD	60.8	1362	46	SEG24	2821.2	1490
10	VLCD	60.8	1234	47	SEG25	2821.2	1618
11	IRQB	60.8	1106	48	SEG26	2821.2	1746
12	IND_BZ	60.8	978	49	SEG27	2821.2	1874
13	EL_BZB	60.8	850	50	SEG28	2821.2	2002
14	COM0	60.8	316.8	51	SEG29	2821.2	2130
15	COM1	60.8	188.8	52	SEG30	2821.2	2258
16	COM2	60.8	60.8	53	SEG31	2821.2	2386
17	COM3	324	60.8	54	SEG32	2342.8	2386
18	COM4	452	60.8	55	SEG33	2214.8	2386
19	COM5	580	60.8	56	SEG34	2086.8	2386
20	COM6	708	60.8	57	SEG35	1958.8	2386
21	COM7	836	60.8	58	SEG36	1830.8	2386
22	SEG0	964	60.8	59	SEG37	1702.8	2386
23	SEG1	1092	60.8	60	SEG38	1574.8	2386
24	SEG2	1220	60.8	61	SEG39	1446.8	2386
25	SEG3	1348	60.8	62	SEG40	1318.8	2386
26	SEG4	1476	60.8	63	SEG41	1190.8	2386
27	SEG5	1604	60.8	64	SEG42	1062.8	2386
28	SEG6	1732	60.8	65	SEG43	934.8	2386
29	SEG7	1860	60.8	66	SEG44	806.8	2386
30	SEG8	1988	60.8	67	SEG45	678.8	2386
31	SEG9	2116	60.8	68	SEG46	550.8	2386
32	SEG10	2244	60.8	69	SEG47	422.8	2386
33	SEG11	2372	60.8				

34	SEG12	2500	60.8				
35	SEG13	2821.2	60.8				
36	SEG14	2821.2	188.8				
37	SEG15	2821.2	316.8		LOGO	1220	1504

History

Date	Name	Version	Comment
2004/2/4	CC Kuo	1.0	Initial
2004/4/29	CC Kuo	1.1	
2004/4/29	CC Kuo	1.2	PAD location and EL_EN function
2005/5/10	Lisa	1.3	Modify the Operating voltage
2005/6/17	Lisa	1.4	Update timing diagram and modify the Operating voltage
2005/6/17	Rong	1.5	Modify command index and timing diagram