# SL3208 Data sheet description Ver2.7

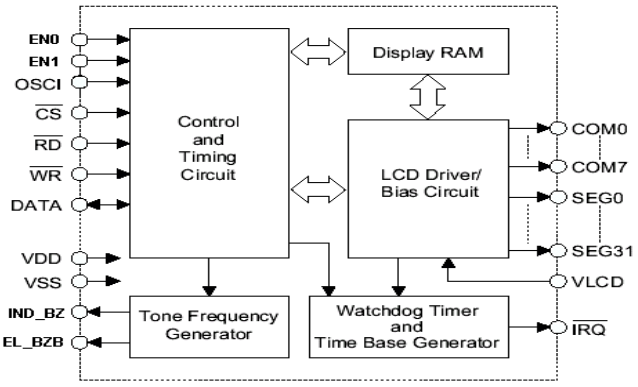
## Features

- Operating voltage: 2.4V~5.2V
- Built-in RC oscillator
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 32x8 patterns, 8 commons, 32 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base/WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Cascade application
- EL application (Only available by internal RC oscillator)
- The frequency outputs of this LCD driver are based on 3.3V power supply.

## General Description

SL3208 is a peripheral device specially designed for I/O type Micro-C used to expand the display capability. The max display segments of the device are 256 patterns (32x8). It also supports serial interface, buzzer sound, Watchdog Timer or time base timer functions. The SL3208 is a memory mapping and multi-function LCD controller. The software configuration features of the SL3208 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the SL3208.

### Block Diagram




Note: CSB: Chip selection
IND_BZ, EL_BZB: Tone outputs/EL application
WRB, RDB, DATA: Serial interface
COM0~COM7, SEG0~SEG31: LCD outputs

## ● Pad Description

| Pad No. | Pad Name | I/O | Function |
|---|---|---|---|
| 1 | CSB | I | Chip selection input with pull high resistor When the CS is logic high, the data and command read from or written to the SL3208 are disabled. The serial interface circuit is also reset. But if CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the SL3208 are all enabled. |
| 2 | EN0 | I | EL/Buzzer function selection input. |
| 3 | RDB | I | READ clock input with pull high resistor Data in the RAM of the SL3208 are clocked out on the falling edge of the RD signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data. |
| 4 | WRB | I | WRITE clock input with pull high resistor Data on the DATA line are latched into the SL3208 on the rising edge of the WR signal. |
| 5 | DATA | I/O | Serial data input/output with pull high resistor |
| 6 | VSS | - | Negative power supply, ground |
| 7 | OSCI | I | The OSCI and OSCO pads are connected to a 32.768KHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open. |
| 8 | OSCO | O | |
| 9 | VDD | -- | Positive power supply |
| 10 | VLCD | I | VLCD POWER INPUT |
| 11 | IRQB | O | Time base or WDT overflow flag, NMOS open drain output |
| 12,14 | IND_BZ, EL_BZB | O | 2KHz or 4KHz tone frequency output pair, EL function output. |
| 13 | EN1 | I | EL/Buzzer function selection input. |
| 15~22 | COM0~COM7 | O | LCD common outputs |
| 23~57 | SEG31~SEG0 | O | LCD segment outputs |

## ●Absolute Maximum Ratings

Supply Voltage……–0.3V ~ 5.5V

Input Voltage……VSS-0.3V ~ VDD+0.3V

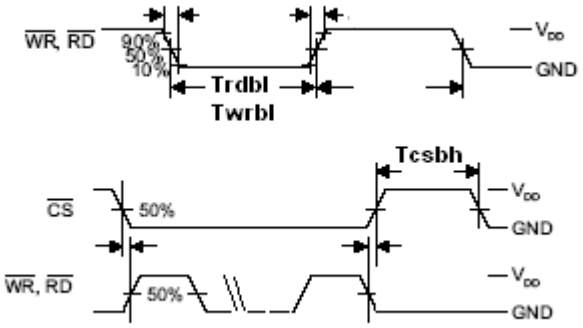
Storage Temperature……..-50°C ~ 125°C

Operating Temperature……-25°C ~ 75°C

## ● DC Character

| Symbol | Parameter | Test Conditions | | Min | Typ. | Max | Unit. |
|---|---|---|---|---|---|---|---|
| | | VDD | Conditions | | | | |
| $I_{stb5}$ | Standby Current | 5V | No load<br>Power down mode | | 5 | 10 | μA |
| $I_{stb3}$ | Standby Current | 3V | No load<br>Power down mode | | 2 | 4 | μA |
| $I_{op5}$ | Operation current | 5V | No load, internal RC oscillator on | | 140 | | μA |
| $I_{op3}$ | Operation current | 3V | No load, internal RC oscillator on | | 60 | | μA |
| $I_{o1}$ | LCD Common Sink Current | 5V | VOL=0V and short to 5V | | 1.9 | | mA |
| $I_{o2}$ | LCD Common Source Current | 5V | VOH=5V and short to 0V | | -3.4 | | mA |
| $I_{o3}$ | LCD Segment Sink Current | 5V | VOL=0V and short to 5V | | 1.91 | | mA |
| $I_{o4}$ | LCD Segment Source Current | 5V | VOH=5V and short to 0V | | -3.5 | | mA |

## ● AC Character

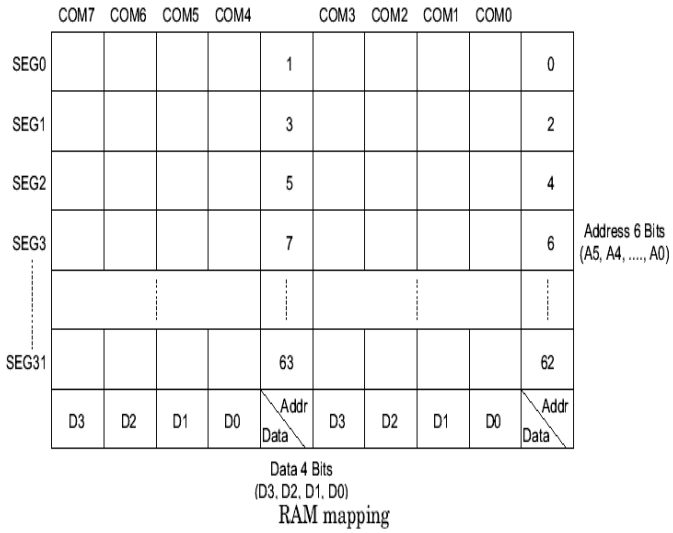



| Symbol | Parameter | Vdd | Min | Typ. | Max | Unit. |
|---|---|---|---|---|---|---|
| $F_{int3}$ | Internal RC oscillator | 3V | | 226 | | KHz |
| $F_{int5}$ | Internal RC oscillator | 5V | | 430 | | KHz |
| $F_{ext5}$ | External input clock | 5V | | | 150 | KHz |
| $T_{rdbl3}$ | Minimum read low pulse | 3V | 350 | | | ns |
| $T_{rdbl5}$ | Minimum read low pulse | 5V | 350 | | | ns |
| $T_{wrbl3}$ | Minimum write low pulse | 3V | 350 | | | ns |
| $T_{wrbl5}$ | Minimum write low pulse | 5V | 350 | | | ns |
| $T_{csbh5}$ | Minimum CSB high pulse | 5V | 50 | | | ns |

# ● Functional Description

## Display Memory RAM

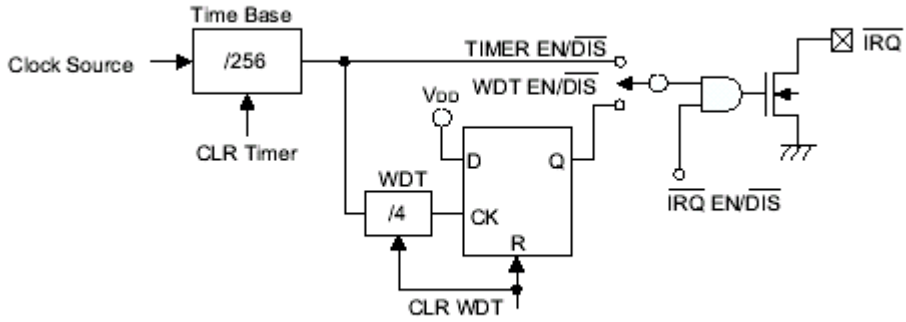
The static display RAM is organized into 64x4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.



RAM mapping

## Time Base and Watchdog Timer (WDT)

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and IRQ EN/DIS are independent from each other. Once the WDT time-out occurs, the IRQ pin will remain at logic low level until the CLR WDT or the IRQ DIS command is issued. If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.




Timer and WDT configurations

## Tone Output

A simple tone generator is implemented in the SL3208. The tone generator can output a pair of differential driving signals on the IND_BZ and EL_BZB which are used to generate a single tone.

## Command Format

The SL3208 can be configured by the software. There are two mode commands to configure the SL3208 resource and to transfer the LCD display data.

| Operation | Mode | ID |
|---|---|---|
| READ | Data | 1 1 0 |
| WRITE | Data | 1 0 1 |
| READ-MODIFY-WRITE | Data | 1 0 1 |
| COMMAND | Command | 1 0 0 |

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in a non-successive command or a non-successive address data mode, the CS pin should be set to "1" and the previous operation mode will be reset also. The CS pin returns to "0", a new operation mode ID should be issued first.

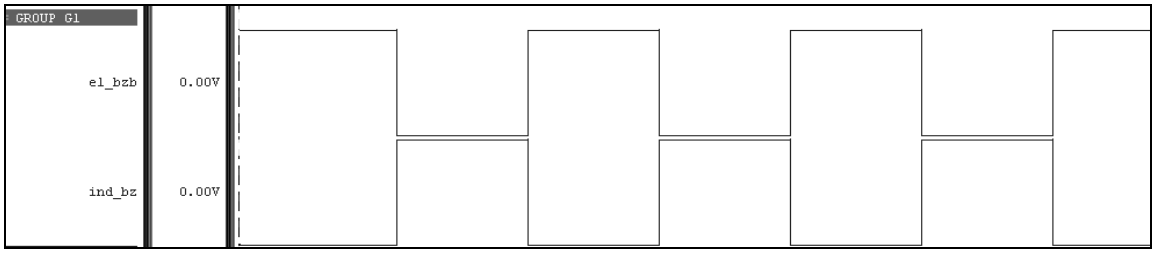
## EL Function

IND_BZ and EL_BZB are multi-functioned as part of EL application circuit by programming EN[1:0]. Four modes are available in this chip…

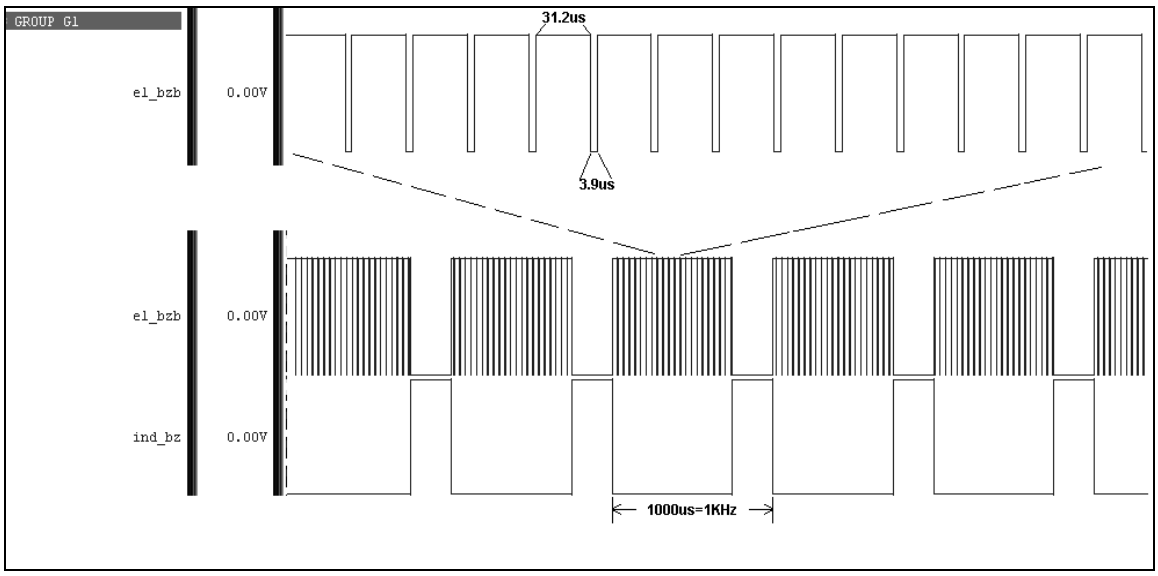
| MODE | EN[1:0] | Function |
|---|---|---|
| MODE[0] | EN1: 0 EN0: 0 | Function as Buzzer. Buzzer output will have 5 seconds delay after turning off. |
| MODE[1] | EN1: 0 EN0: 1 | 5-second delay of EL frequency output after "**TONE OFF**" command is issued. Before issuing TONE OFF command, EL frequency output is determined by two commands, that is …"**TONE 2K**" and "**TONE 4k**".<br>For TONE 2K, the EL output frequency will be 500Hz<br>For TONE 4K, the EL output frequency will be 1KHz |
| MODE[2] | EN1: 1 EN0: 0 | Continuous 500Hz EL frequency output |
| MODE[3] | EN1: 1 EN0: 1 | Continuous 1KHz EL frequency output |

Note : Only available by internal RC oscillator

Buzzer waveform at (Mode 0):

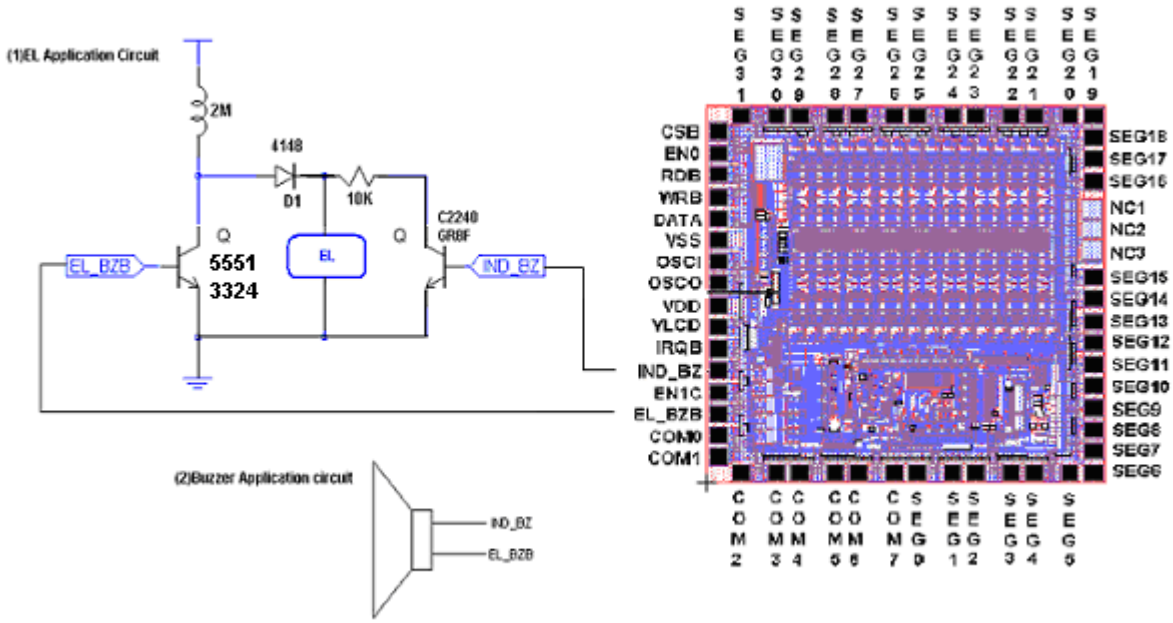



1KHz EL frequency output waveform at (Mode 1, 2 and 3):

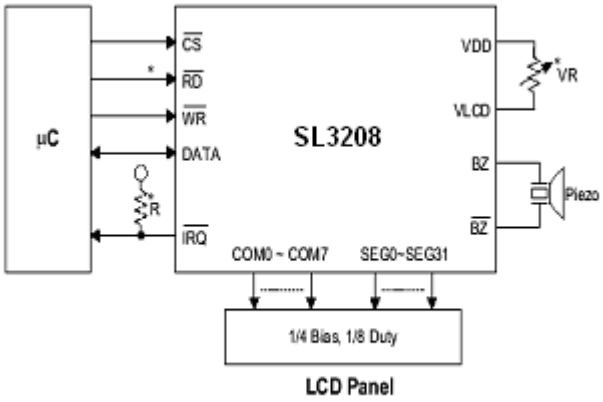



During charge period, the voltage at anode of diode (DN4148) is about 100V.

## EL Application Circuit




## ● Application Circuit



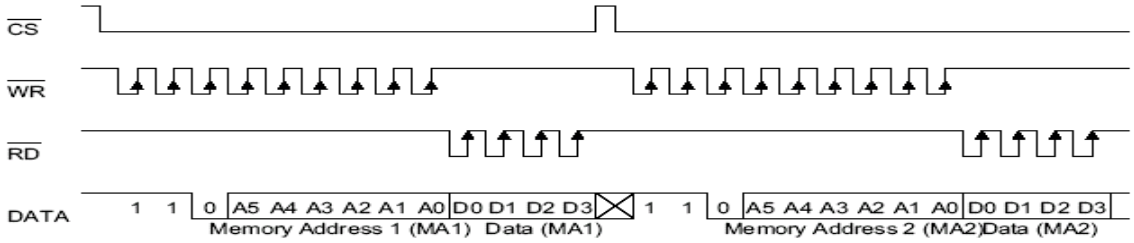

Host controller with a SL3208 display system

Note: The connection of IRQ and RD pin can be selected depending on the requirement of the Micro-C. The voltage applied to $V_{LCD}$ pin must be lower than $V_{DD}$. Adjust VR to fit LCD display, at $V_{DD}$=5V, $V_{LCD}$=4V, VR about 20k. Adjust R (external pull-high resistance) to fit user s time base clock.

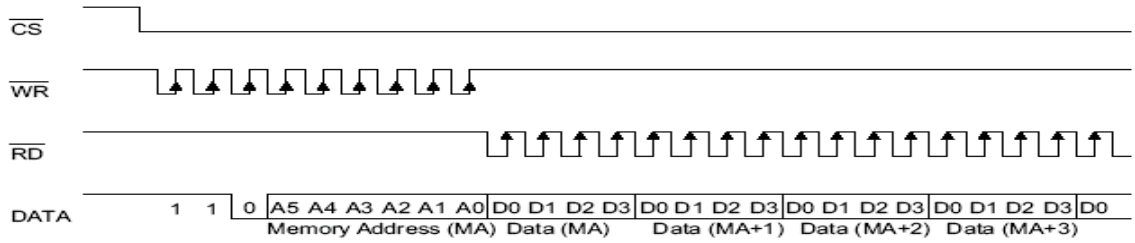
## ● Timing Diagram

**Timing Diagrams**

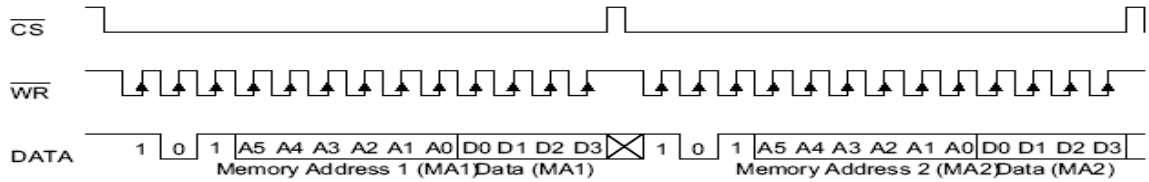
**READ mode (command code : 1 1 0)**



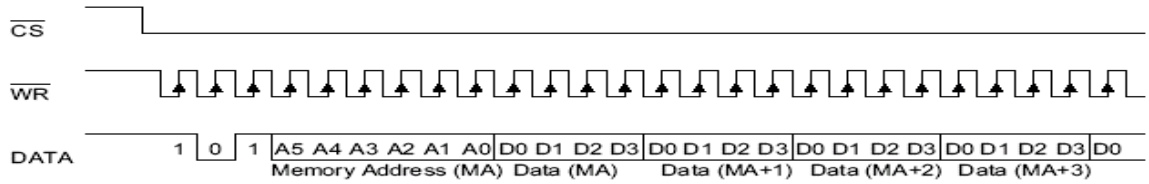

**READ mode (successive address reading)**



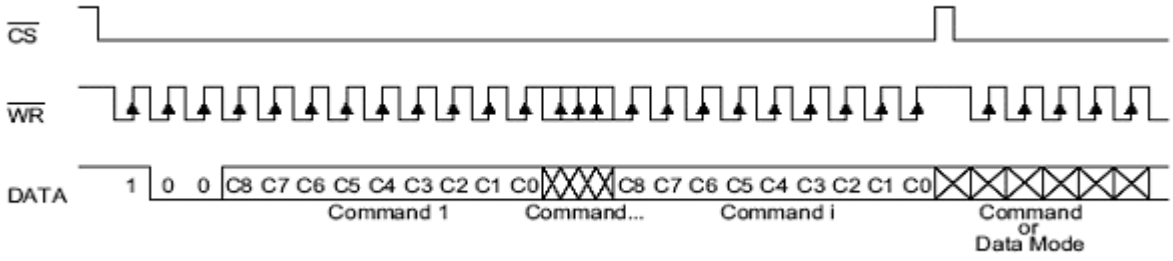

**WRITE mode (command code : 1 0 1)**




**WRITE mode (successive address writing)**




**Command mode (command code : 1 0 0)**



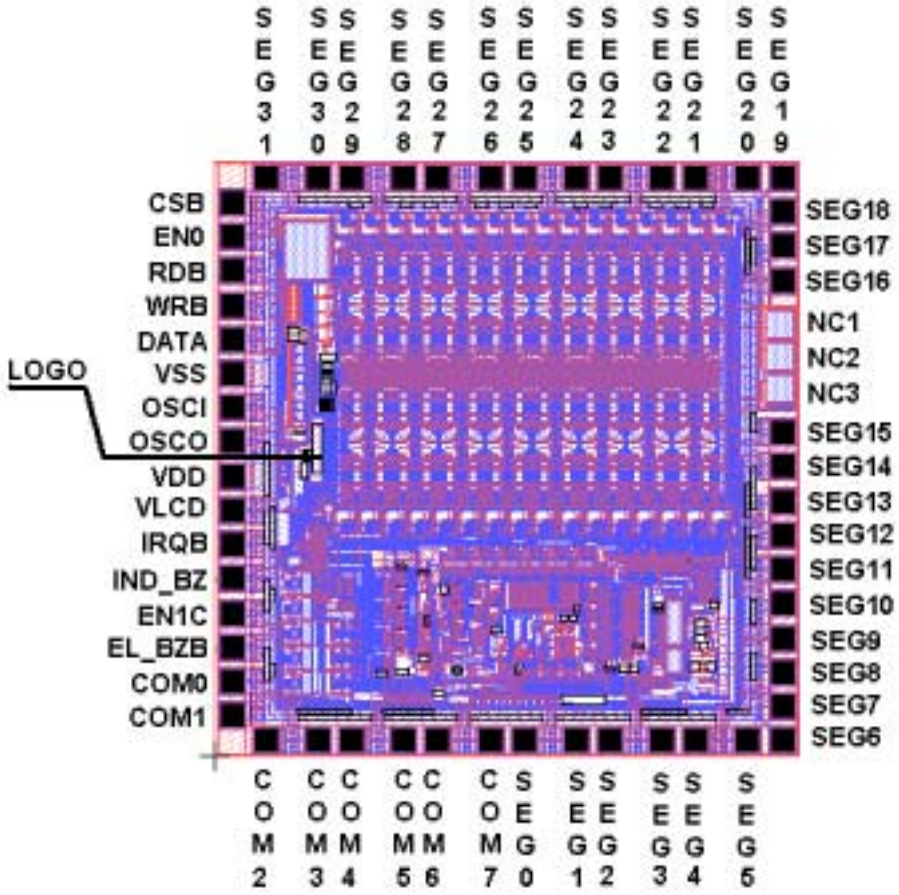
## ● Command Index

| Name | ID | Command Code | D/C | Function | Def. |
|---|---|---|---|---|---|
| READ | 1 1 0 | A5A4A3A2A1A0D0D1D2D3 | D | Read data from the RAM | |
| WRITE | 1 0 1 | A5A4A3A2A1A0D0D1D2D3 | D | Write data to the RAM | |
| READ- MODIFY-WRITE | 1 0 1 | A5A4A3A2A1A0D0D1D2D3 | D | READ and WRITE to the RAM | |
| SYS DIS | 1 0 0 | 0000-0000-X | C | Turn off both system oscillator and LCD bias generator | Yes |
| SYS EN | 1 0 0 | 0000-0001-X | C | Turn on system oscillator | |
| LCD OFF | 1 0 0 | 0000-0010-X | C | Turn off LCD bias generator | Yes |
| LCD ON | 1 0 0 | 0000-0011-X | C | Turn on LCD bias generator | |
| TIMER DIS | 1 0 0 | 0000-0100-X | C | Disable time base output | |
| WDT DIS | 1 0 0 | 0000-0101-X | C | Disable WDT time-out flag output | |
| TIMER EN | 1 0 0 | 0000-0110-X | C | Enable time base output | |
| WDT EN | 1 0 0 | 0000-0111-X | C | Enable WDT time-out flag output | |
| TONE OFF | 1 0 0 | 0000-1000-X | C | Turn off tone outputs | Yes |
| TONE ON | 1 0 0 | 0000-1001-X | C | Turn on tone outputs | |
| CLR TIMER | 1 0 0 | 0000-1101-X | C | Clear the contents of time base generator | |
| CLR WDT | 1 0 0 | 0000-1111-X | C | Clear the contents of WDT stage | |
| RC 256K | 1 0 0 | 0001-10XX-X | C | System clock source, on chip RC oscillator | Yes |
| EXT 32K | 1 0 0 | 0001-11XX-X | C | System clock source, external clock source | |
| TONE 4K | 1 0 0 | 010X-XXXX-X | C | Tone frequency, 4KHz | |
| TONE 2K | 1 0 0 | 011X-XXXX-X | C | Tone frequency, 2KHz | |
| IRQ DIS | 1 0 0 | 100X-0XXX-X | C | Disable IRQ output | Yes |
| IRQ EN | 1 0 0 | 100X-1XXX-X | C | Enable IRQ output | |
| F1 | 1 0 0 | 101X-X000-X | C | Time base/WDT clock output:1Hz<br>The WDT time-out flag after: 4s | |
| F2 | 1 0 0 | 101X-X001-X | C | Time base/WDT clock output:2Hz The WDT time-out flag after: 2s | |
| F4 | 1 0 0 | 101X-X010-X | C | Time base/WDT clock output:4Hz<br>The WDT time-out flag after: 1s | |
| F8 | 1 0 0 | 101X-X011-X | C | Time base/WDT clock Output: 8Hz<br>The WDT time-out flag after: 1/2 s | |
| F16 | 1 0 0 | 101X-X100-X | C | Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4 s | |
| F32 | 1 0 0 | 101X-X101-X | C | Time base/WDT clock output: 32Hz<br>The WDT time-out flag after: 1/8 s | |
| F64 | 1 0 0 | 101X-X110-X | C | Time base/WDT clock output:64Hz<br>The WDT time-out flag after: 1/16 s | |
| F128 | 1 0 0 | 101X-X111-X | C | Time base/WDT clock output:128Hz<br>The WDT time-out flag after: 1/32 s | Yes |

Note: X: Don't care
A5~A0: RAM addresses
D3~D0: RAM data
D/C: Data/command mode
Def.: Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SL3208 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SL3208.

## Pin Assignment




The IC substrate should be connected to VDD in the PCB layout artwork.

## ● Pad Coordinates

| No. | Pin Name | X | Y | No. | Pin Name | X | Y |
|---|---|---|---|---|---|---|---|
| 1 | CSB | 76 | 2592.5 | 30 | SEG7 | 2648 | 236 |
| 2 | EN0 | 76 | 2432.5 | 31 | SEG8 | 2648 | 396 |
| 3 | RDB | 76 | 2272.5 | 32 | SEG9 | 2648 | 556 |
| 4 | WRB | 76 | 2112.5 | 33 | SEG10 | 2648 | 716 |
| 5 | DATA | 76 | 1952.5 | 34 | SEG11 | 2648 | 876 |
| 6 | VSS | 76 | 1792.5 | 35 | SEG12 | 2648 | 1036 |
| 7 | OSCI | 76 | 1632.5 | 36 | SEG13 | 2648 | 1196 |
| 8 | OSCO | 76 | 1472.5 | 37 | SEG14 | 2648 | 1356 |
| 9 | VDD | 76 | 1312.5 | 38 | SEG15 | 2648 | 1516 |
| 10 | VLCD | 76 | 1152.5 | 39 | NC1 | 2626 | 1720 |
| 11 | IRQB | 76 | 992.5 | 40 | NC2 | 2626 | 1870 |
| 12 | IND_BZ | 76 | 832.5 | 41 | NC3 | 2626 | 2011 |
| 13 | EN1 | 76 | 672.5 | 42 | SEG16 | 2648 | 2229 |
| 14 | EL_BZB | 76 | 512.5 | 43 | SEG17 | 2648 | 2389 |
| 15 | COM0 | 76 | 352.5 | 44 | SEG18 | 2648 | 2549 |
| 16 | COM1 | 76 | 192.5 | 45 | SEG19 | 2648 | 2709 |
| 17 | COM2 | 236 | 76 | 46 | SEG20 | 2488 | 2709 |
| 18 | COM3 | 478 | 76 | 47 | SEG21 | 2246 | 2709 |
| 19 | COM4 | 638 | 76 | 48 | SEG22 | 2086 | 2709 |
| 20 | COM5 | 880 | 76 | 49 | SEG23 | 1844 | 2709 |
| 21 | COM6 | 1040 | 76 | 50 | SEG24 | 1684 | 2709 |
| 22 | COM7 | 1282 | 76 | 51 | SEG25 | 1442 | 2709 |
| 23 | SEG0 | 1442 | 76 | 52 | SEG26 | 1282 | 2709 |
| 24 | SEG1 | 1684 | 76 | 53 | SEG27 | 1040 | 2709 |
| 25 | SEG2 | 1844 | 76 | 54 | SEG28 | 880 | 2709 |
| 26 | SEG3 | 2086 | 76 | 55 | SEG29 | 638 | 2709 |
| 27 | SEG4 | 2246 | 76 | 56 | SEG30 | 478 | 2709 |
| 28 | SEG5 | 2488 | 76 | 57 | SEG31 | 236 | 2709 |
| 29 | SEG6 | 2648 | 76 | 58 | LOGO | 476.5 | 1440.5 |

## ● History

| Date | Name | Version | Comment |
|---|---|---|---|
| 2003/2/10 | CC Kuo | 1.0 | Initial |
| 2003/2/13 | CC Kuo | 1.1 | |
| 2003/2/26 | CC Kuo | 1.2 | |
| 2003/5/20 | CC Kuo | 1.3 | |
| 2003/6/11 | CC Kuo | 1.4 | |
| 2003/7/09 | CC Kuo | 1.5 | Modified the DC spec and Timing diagram and Pad coordinates |
| 2003/7/10 | CC Kuo | 1.6 | Modified the DC spec. |
| 2003/8/25 | CC Kuo | 1.7 | Modified the DC spec. |
| 2003/8/29 | CC Kuo | 1.8 | Modified power supply voltage |
| 2003/9/05 | CC Kuo | 2.0 | Create SL3208 |
| 2003/9/20 | CC Kuo | 2.1 | Add the AC timing spec. |
| 2004/2/24 | CC Kuo | 2.2 | Modify the AC spec. |
| 2004/7/19 | CCKuo | 2.3 | Modify the pin location |
| 2005/3/23 | Lisa | 2.4 | Add the DC Absolute Maximum Ratings |
| 2005/5/10 | Lisa | 2.5 | Modify the Operating voltage |
| 2005/5/13 | Rong | 2.6 | Modify the pin location |
| 2005/6/17 | Lisa | 2.7 | Update timing diagram and modify the Operating voltage |