SL3204 Data sheet description Ver4.3

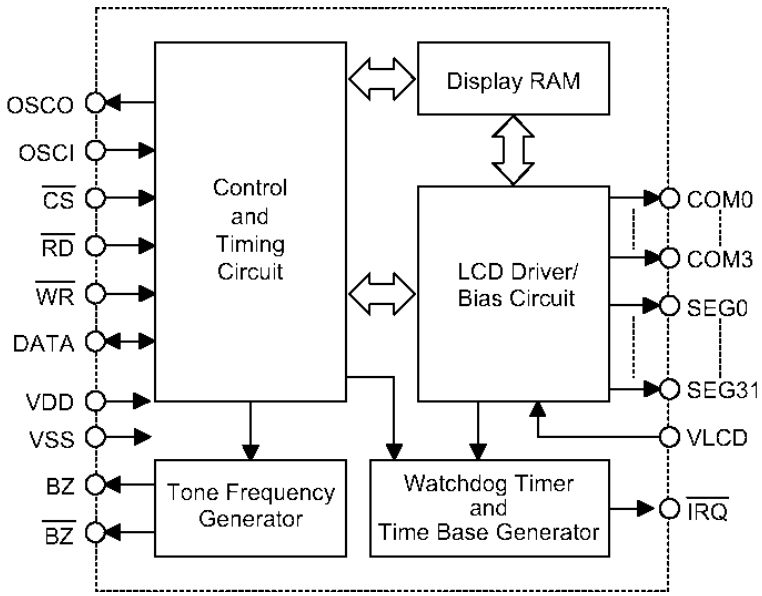
Features

- Operating voltage : 2.4V~5.2V
- Built-in 256KHz RC oscillator
- External 32.768KHz crystal or 256KHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2KHz/4KHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32x4 LCD driver
- Built-in 32x4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage

General Description

The SL3204 is a 128 patterns (32x4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the SL3204 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the SL3204. The SL3204 contains a power down command to reduce power consumption.

Block Diagram



Note: CSB: Chip selection
BZ, BZB: Tone outputs
WRB, RDB, DATA: Serial interface
COM0~COM3, SEG0~SEG31: LCD outputs
IRQB: Time base or WDT overflow output

● Pad Description

Pad No.	Pad Name	I/O	Function
1	CSB	I	Chip selection input with pull high resistor When the CS is logic high, the data and command read from or written to the SL3204are disabled. The serial interface circuit is also reset. But if CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the SL3204 are all enabled.
2	RDB	I	READ clock input with pull high resistor Data in the RAM of the SL3204 are clocked out on the falling edge of the RD signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	WRB	I	WRITE clock input with pull high resistor Data on the DATA line are latched into the SL3204on the rising edge of the WR signal.
4	DATA	I/O	Serial data input/output with pull high resistor
5	VSS	-	Negative power supply, ground
6	OSCO	O	The OSCI and OSCO pads are connected to a 32.768KHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
7	OSCI	I	
8	VLCD	I	LCD power input
9	VDD	-	Positive power supply
10	IRQB	O	Time base or WDT overflow flag, NMOS open drain output
11~12	BZ,BZB	O	2KHz or 4KHz tone frequency output pair
13~16	COM0~COM3	O	LCD common outputs
17~48	SEG31~SEG0	O	LCD segment outputs

4- - Absolute Maximum Ratings

Supply Voltage……–0.3V ~ 5.5V

Input Voltage……VSS-0.3V ~ VDD+0.3V

Storage Temperature……..-50°C ~ 125°C

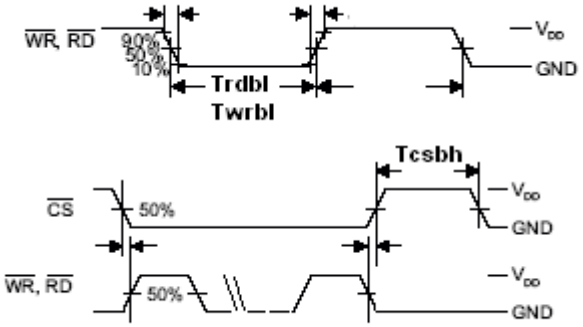
Operating Temperature……-25°C ~ 75°C

● DC Characteristic

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit.
		VDD	Conditions				
Istb1	Standby Current	5V	No load Power down mode	-	5	-	uA
Istb2	Standby Current	3v	No load Power down mod		2		uA
Idd1	Operation current	5v	No load, internal RC oscillator on		120		uA
Idd2	Operation current	3v	No load, internal RC oscillator on		48		uA
I_{O1}	LCD Common Sink Current	5V	VOL=2.5V		2.36		mA
I_{O2}	LCD Common Source Current	5V	VOH=2.5V		1.51		mA
I_{O3}	LCD Segment Sink Current	5V	VOL=2.5V		1.58		mA
I_{O4}	LCD Segment Source Current	5V	VOH=2.5V		0.9		mA

● AC Character

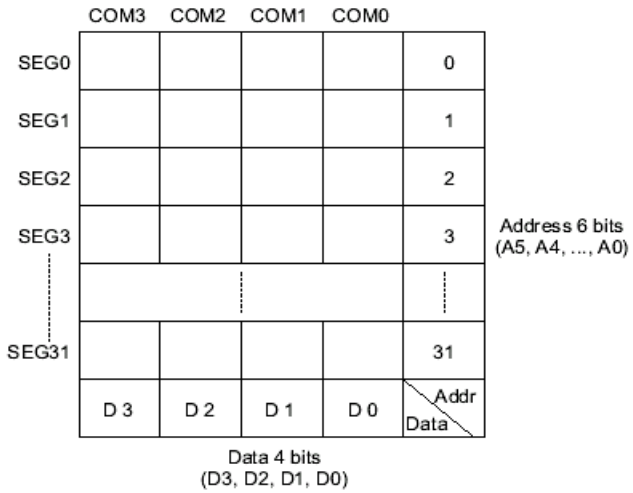


Symbol	Parameter	Vdd	Min	Typ.	Max	Unit.
F_{int3}	Internal RC oscillator	3V		133		KHz
F_{int5}	Internal RC oscillator	5V		256		KHz
F_{ext5}	External input clock	5V			3.5	MHz
T_{rdbl3}	Minimum read low pulse	3V	350			ns
T_{rdbl5}	Minimum read low pulse	5V	350			ns
T_{wrbl3}	Minimum write low pulse	3V	350			ns
T_{wrbl5}	Minimum write low pulse	5V	350			ns
T_{csbh5}	Minimum CSB high pulse	5V	50			ns

● Functional Description

Display Memory RAM

The static display memory (RAM) is organized into 32x4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern



RAM mapping

System Oscillator

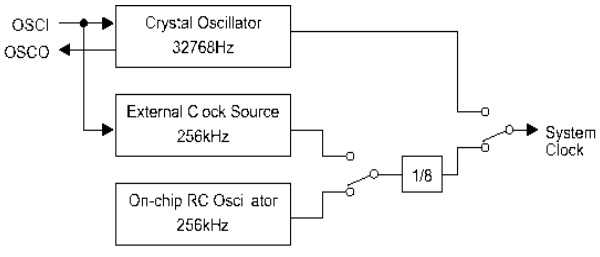
The SL3204 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on chip RC oscillator (256 KHz), a crystal oscillator (32.768 KHz), or an external 256 KHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32 KHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256 KHz clock source operation.

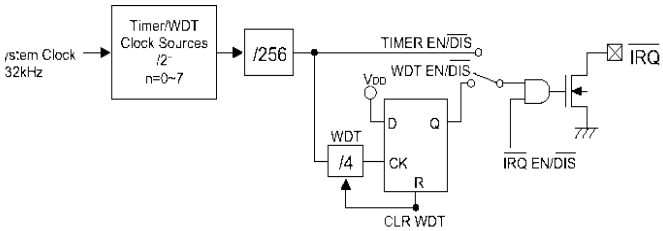
At the initial system power on, the SL3204 is at the SYS DIS state.

Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8 stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8 stage time base generator along with a 2 stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time out will result in the setting of an internal WDT time out flag. The outputs of the time base generator and of the WDT time out flag can be connected to the IRQ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation. $f_{WDT} = \frac{32KHz}{2^n}$ Where the value of n ranges from 0 to 7 by command options. The 32 KHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768 KHz, an on chip oscillator (256 KHz), or an external frequency of 256 KHz. If an on chip oscillator (256 KHz) or an external 256 KHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32 KHz by a 3 stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8 stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time out flag output (connect the WDT time out flag to the IRQ pin). After the TIMER EN command is transferred, the WDT is disconnected from the IRQ pin, and the output of the time base generator is connected to the IRQ pin. The WDT can be cleared by executing the CLR WDT command and the contents of the time base generator is cleared by executing the CLR TIMER command.



System oscillatoe configuration



Timer and WDT configuration

Name	Command Code	Function
LCD OFF	10000000010X	Turn off LCD outputs
LCD ON	10000000011X	Turn on LCD outputs
BIAS & COM	1000010abXcX	C=0 : 1/2 bios option C=1 : 1/3 bios option Ab=00 : 2 commons option Ab=01 : 3 commons option Ab=10 : 4 commons option

The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the IRQ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time out occurs, the IRQ pin will stay at a logic low level until the CLR WDT or the IRQ DIS command is issued. After the IRQ output is disabled the IRQ pin will remain at the floating state. The IRQ output can be enabled or disabled by executing the IRQ EN or the IRQ DIS command, respectively. The IRQ EN makes the output of the time base generator or of the WDT time out flag appear on the IRQ pin. The configuration of the time base generator along with the WDT is as shown. In the case of on chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions. On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the SL3204 will continue working until system power fails or the external clock source is removed. After the system power on, the IRQ will be disabled.

Tone Output

A simple tone generator is implemented in the SL3204. The tone generator can output a pair of differential driving signals on the BZ and BZB, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4 KHz and 2 KHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and BZB, are a pair of differential driving outputs used to drive a buzzer.

LCD Driver

The SL3204 is a 128 (32x4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the SL3204 suitable for multiple LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768 KHz crystal oscillator frequency, an on chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table. The bold form of 1 0 0, namely 1 0 0, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands; the SL3204 can be compatible with most types of LCD panels.

Command Format

The SL3204 can be configured by the S/W setting. There are two mode commands to configure the SL3204 resources and to transfer the LCD display data. The configuration mode of the SL3204 is called command mode, and its command mode ID is 1 0 0. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode Ids and the command mode ID:

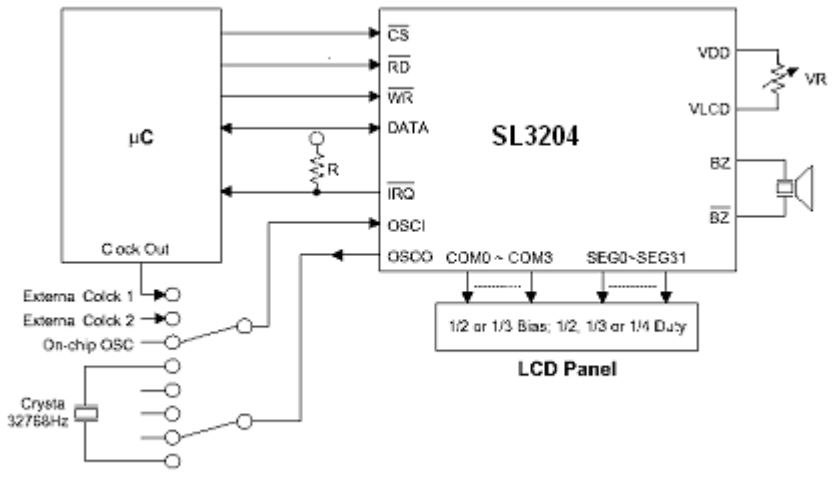
Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 1 0 0, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CS pin should be set to “1” and the previous operation mode will be reset also. Once the CS pin returns to “0” a new operation mode ID should be issued first.

Interfacing

Only four lines are required to interface with the SL3204. The CS line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the SL3204. If the CS pin is set to “1”, the data and command issued between the host controller and the SL3204 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the SL3204. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The RD line is the READ clock input. Data in the RAM are clocked out on the falling edge of the RD signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the RD signal. The WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the SL3204 on the rising edge of the WR signal. There is an optional IRQ line to be used as an interface between the host controller and the SL3204. The IRQ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the IRQ pin of the SL3204.

Application Circuit



Host controller with a SL3204 display system

Note: See next page for notes.

Note: The connection of IRQB and RDB pin can be selected depending on the requirement of the up

The voltage applied to V_{LCD} pin must be lower then V_{DD}.

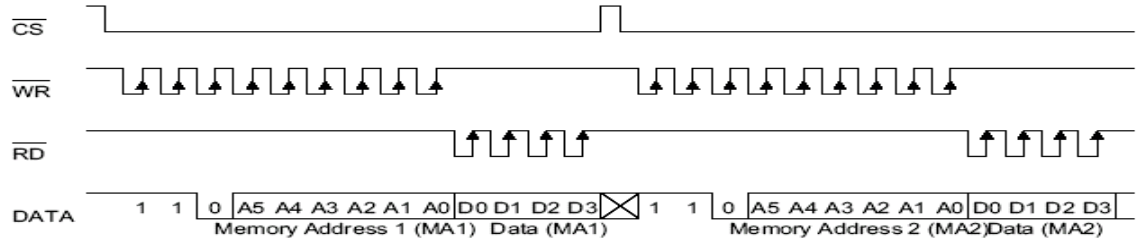
Adjust VR to fit LCD display, at V_{DD} = 5V, V_{LCD} = 4V, VR = 15Kohm +/- 20%.

Adjust R to fit user's time base clock.

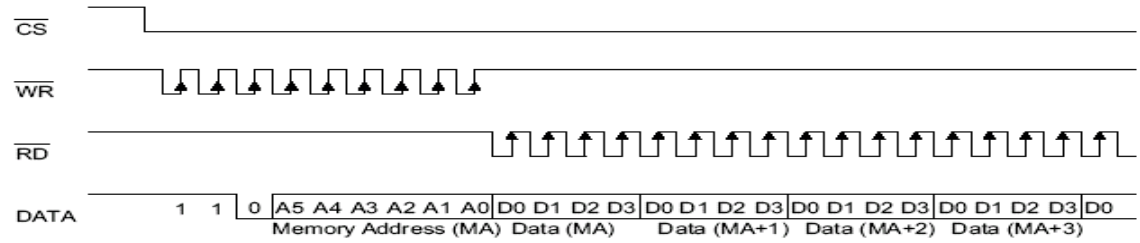
● Timing Diagram

Timing Diagrams

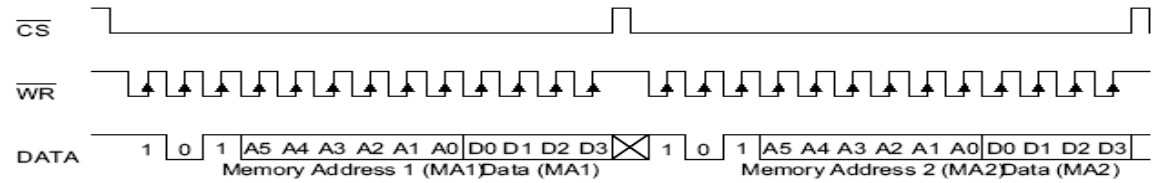
READ mode (command code : 1 1 0)



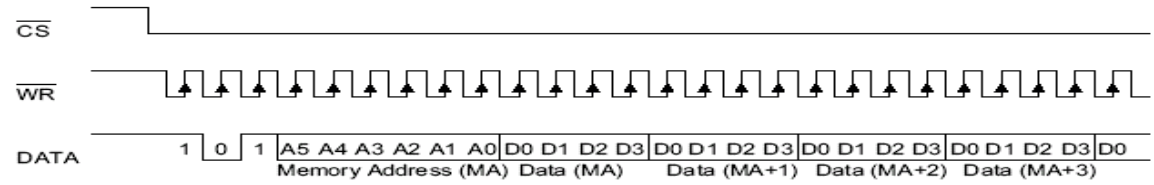
READ mode (successive address reading)



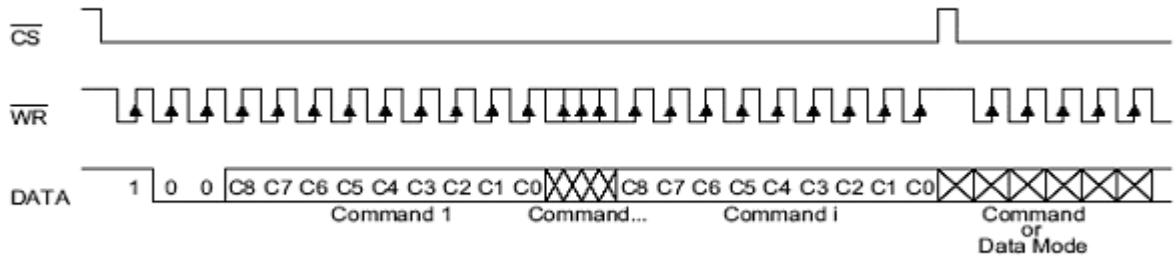
WRITE mode (command code : 1 0 1)



WRITE mode (successive address writing)



Command mode (command code : 1 0 0)



● Command Index

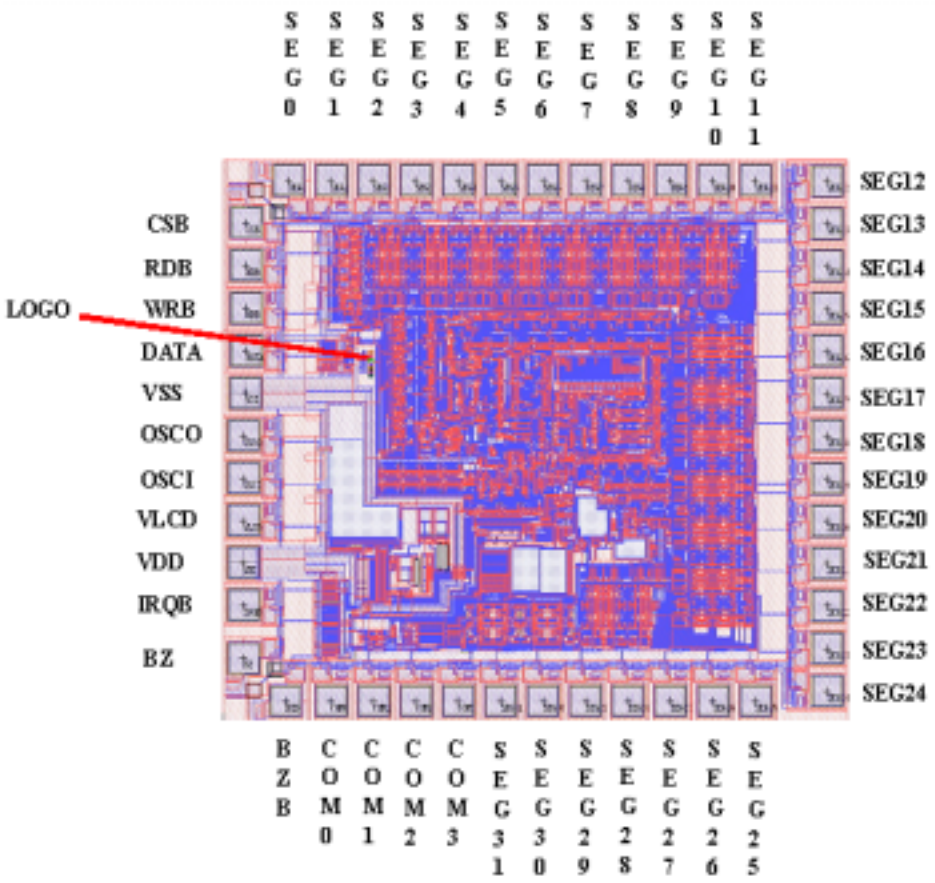
Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	1 0 0	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	1 0 0	0000-1101-X	C	Clear the contents of time base generator	
CLR WDT	1 0 0	0000-1111-X	C	Clear the contents of WDT stage	
XTAL 32K	1 0 0	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	1 0 0	0001-10XX-X	C	System clock source, on chip RC oscillator	Yes
EXT 256K	1 0 0	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	1 0 0	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	1 0 0	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	1 0 0	010X-XXXX-X	C	Tone frequency, 4KHz	
TONE 2K	1 0 0	011X-XXXX-X	C	Tone frequency, 2KHz	
IRQ DIS	1 0 0	100X-0XXX-X	C	Disable IRQ output	Yes
IRQ EN	1 0 0	100X-1XXX-X	C	Enable IRQ output	
F1	1 0 0	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	1 0 0	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	1 0 0	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	

F8	1 0 0	101X-X011-X	C	Time base/WDT clock Output: 8Hz The WDT time-out flag after: 1/2 s	
F16	1 0 0	101X-X100-X	C	Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4 s	
F32	1 0 0	101X-X101-X	C	Time base/WDT clock output: 32Hz The WDT time-out flag after: 1/8 s	
F64	1 0 0	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16 s	
F128	1 0 0	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32 s	Yes
TEST	1 0 0	1110-0000-X	C	Test mode, user don't use.	
NORMA L	1 0 0	1110-0011-X	C	Normal mode	Yes

Note: X: Don't care
A5~A0: RAM addresses
D3~D0: RAM data
D/C: Data/command mode
Def.: Power on reset default

All the bold forms, namely 1 1 0, 1 0 1, and 1 0 0, are mode commands. Of these 1 0 0 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on chip 256KHz RC oscillator, a 32.768 KHz crystal oscillator, or an external 256KHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SL3204 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SL3204.

Pin Assignment

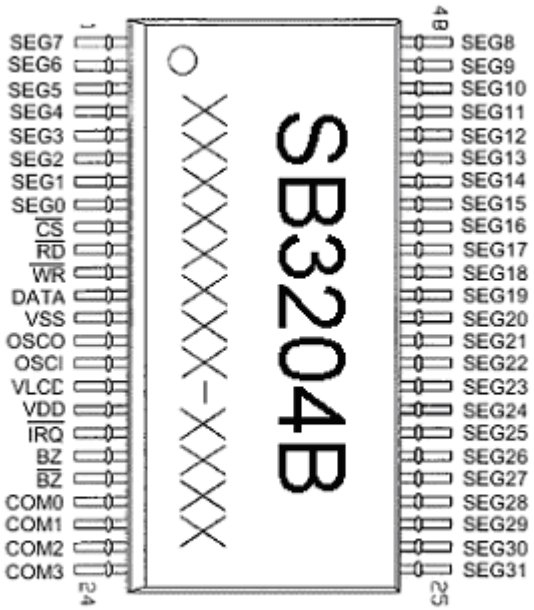


● Pad Coordinates

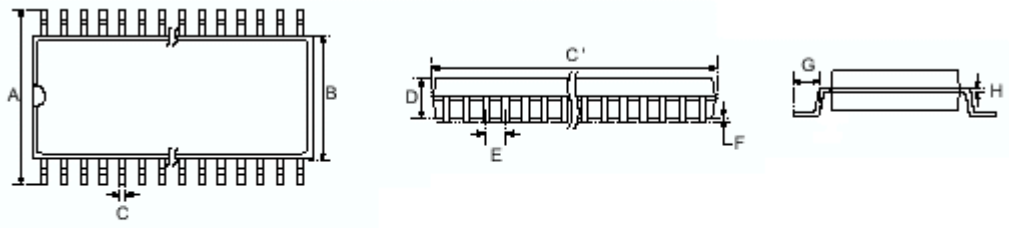
No.	Name	x	y	No.	Name	x	Y
1	CSB	68.80	1499.44	25	SEG23	1820.80	218.24
2	RDB	68.80	1371.44	26	SEG22	1820.80	346.24
3	WRB	68.80	1243.44	27	SEG21	1820.80	474.24
4	DATA	68.80	1115.44	28	SEG20	1820.80	602.24
5	VSS	68.80	987.44	29	SEG19	1820.80	730.24
6	OSCO	60.80	859.44	30	SEG18	1820.80	858.24
7	OSCI	60.80	731.44	31	SEG17	1820.80	986.24
8	VLCD	60.80	603.44	32	SEG16	1820.80	1114.24
9	VDD	60.80	475.44	33	SEG15	1820.80	1242.24
10	IRQB	60.80	348.24	34	SEG14	1820.80	1370.24
11	BZ	60.80	188.80	35	SEG13	1820.80	1498.24
12	BZB	188.88	60.80	36	SEG12	1820.80	1626.24
13	COM0	324.56	60.80	37	SEG11	1604.80	1627.44
14	COM1	452.56	60.80	38	SEG10	1476.80	1627.44
15	COM2	580.56	60.80	39	SEG9	1348.80	1627.44
16	COM3	708.56	60.80	40	SEG8	1220.80	1627.44
17	SEG31	836.56	60.80	41	SEG7	1092.80	1627.44
18	SEG30	964.56	60.80	42	SEG6	964.80	1627.44
19	SEG29	1092.56	60.80	43	SEG5	836.80	1627.44
20	SEG28	1220.56	60.80	44	SEG4	708.80	1627.44
21	SEG27	1348.56	60.80	45	SEG3	580.80	1627.44
22	SEG26	1476.56	60.80	46	SEG2	452.80	1627.44
23	SEG25	1604.56	60.80	47	SEG1	324.80	1627.44
24	SEG24	1820.80	90.24	48	SEG0	196.80	1627.44
	LOGO	435	1072				

● Package

SSOP 48 Pins



SSOP 48pin



A	B	C	C'	D	E	F	G	H
395~420	291~299	8~12	613~637	85~99	20~30	4~10	25~35	4~12

● History

Date	Name	Version	Comment
2003/2/9	CC Kuo	1.0	Initial
2003/2/13	CC Kuo	1.1	
2003/3/17	CC Kuo	1.2	Insert the package information
2003/5/26	CC Kuo	2.0	
2003/9/05	CC Kuo	3.0	
2003/9/15	CC Kuo	3.1	Modify timing diagram
2003/9/20	CC Kuo	3.2	Add the AC spec
2003/9/25	CC Kuo	3.3	Modify the pin assignment
2003/11/20	CC Kuo	3.4	Add package information
2004/2/24	CC Kuo	3.5	Modify the AC spec.
2005/3/23	Rong	3.6	Add the DC Absolute Maximum Ratings
2005/4/20	Lisa	3.7	Add the D.C.spec
2005/5/10	Lisa	3.8	Modify the Operating voltage
2005/6/8	Lisa	3.9	Modify the command code
2005/6/17	Lisa	4.0	Modify the Operating voltage
2005/7/12	Lisa	4.1	Modify the pin location
2005/11/2	Alec	4.2	Modify index
2005/11/9	Alec	4.3	Modify pin assignment and pin location